Realization of normally-off GaN HEMTs for high voltage and low resistance applications

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Abstract

With the development of power electronics, the replacement of silicon by a promising candidate becomes necessary in the field of high power applications. The GaN-based devices are attractive for the high power switching applications, owing to their superior advantages of high breakdown electrical field, high carrier mobility, and fast switching speed. However, the realization of normally-off GaN-based devices for high voltage and low resistance applications is not fully accomplished. In this thesis, the simulation, fabrication, and characterization of the AlGaN/GaN MIS-HEMTs for improving high-power properties are carried out.

The TCAD simulation was first implemented to understand the effect of gate dielectric parameters and Al_2O_3/GaN interface states on the C–V behavior of AlGaN/GaN MIS-capacitors. After that, an economical and effective method of the 1-Octadecanethiol treatment on the GaN surface prior to the Al_2O_3 gate dielectric deposition proposed to improve the Al_2O_3/GaN interface quality. The GaN-based Metal-Insulator-Semiconductor devices treated by HCl, O_2 plasma and ODT have been demonstrated. The ODT treatment is found capable of suppressing native oxide and also passivating the GaN surface effectively, hence the interface quality of the device is considerably improved. The interface traps density of Al_2O_3/GaN has been calculated to be around $3.0x10^{12}$ $cm^{-2}eV^{-1}$ for devices with the ODT treatment, which is a relatively low value reported using Al_2O_3 for the gate dielectric in GaN-based MIS devices. Moreover, there is also an improvement in the gate control characteristics of MIS-HEMTs fabricated with the ODT treatment.

In addition, a simulation of off-state breakdown voltage and electric field profiles in the MIS-HEMTs as functions of the device structures was carried out. In order to improve the high voltage performances of the devices, the AlGaN/GaN MIS-HEMTs with SiN_x single-layer passivation, Al_2O_3/SiN_x bilayer passivation, and ZrO_2/SiN_x bilayer passivation are investigated. High-*k* dielectrics are adopted as the passivation layer on MIS-HEMTs to suppress the shallow traps on the GaN surface. Besides, high-*k* dielectrics passivated MIS-HEMTs also show improved breakdown characteristics, and that is explained by the 2-D simulation analysis. The fabricated devices with high-*k* dielectrics/SiN_x bilayer passivation exhibit improved power performance than the devices with plasma enhanced chemical vapor deposition-SiN_x single layer passivation, including lower leakage currents, smaller current collapse, and higher breakdown voltage. The Al_2O_3/SiN_x passivated MIS-HEMTs exhibit a breakdown voltage of 1092 V, and the dynamic Ron is only 1.14 times the static Ron after off-state V_{DS} stress of 150 V. On the other hand, the ZrO_2/SiN_x passivated MIS-HEMTs exhibit a higher breakdown voltage of 1203 V, and the dynamic R_{on} is 1.25 times the static R_{on} after off-state V_{DS} stress of 150 V.

Furthermore, in order to realize the GaN-based devices with normally-off operations, the AlGaN/GaN MIS-FET with a fully-recessed gate structure was firstly investigated. The devices exhibited a large on-state resistance, which is not desirable for high power applications. After that, a novel normally-off AlGaN/GaN MIS-HEMTs structure with a ZrO_x trap charging layer is proposed. The deposition of the ZrO_x charge trapping layer on the partially recessed AlGaN in conjunction with the Al_2O_3 gate

dielectric was developed. The fabricated MIS-HEMTs presented a threshold voltage of +1.51 V and a maximum drain current density of 779 mA/mm, which accompanied a low on-resistance of 7 Ω·mm. Moreover, switching after an off-state $V_{DS,Q}$ stress of 200 V, the degradation of dynamic on-resistance was a low value of 1.5, indicating of a satisfactory interface between ZrO_x and GaN. Furthermore, the devices exhibit a high breakdown voltage of 1447 V. Though further improvement is needed on the charges storage stability, the results indicate a significant potential of employing the ALD-ZrO_x charge trapping layer to realize normally-off the GaN-based devices for high power applications.

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List of Symbols

Term	Initial Components of the Terms
β	Weibull slop
BV	Breakdown Voltage
C	Capacitance
C_{ox}	Oxide capacitance
D_{it}	Interface State Density
σ	Capture Cross Section of the Trap States
E_C	Conduction Band
E_F	Fermi Level
E_i	Charge Neutrality Level
E_T	Valance Band
E_{OX}	Electric Field on Oxide
$E_{Trap}(f_m)$	The Detectable Energy of Interface Trap
ε_r	Relative Permittivity
ε_0	Permittivity of vacuum
f	Frequency
f_m	Measurement Frequency
φ_b	Barrier Height
g_m	Transconductance
I_D	Drain Current

I_{DMAX}	Maximum Drain Saturation Current
I_G	Gate Leakage Current
k	Boltzmann Constant
L_{GD}	Gate to Drain Spacing
L_G	Gate Length
L_{SG}	Source to Gate Spacing
N_C	Effective Density of States
q	Elemental Charge
Q_{int}	Interface Fixed Charge
R_C	Contact Resistance
R_{ON}	ON-Resistance
$R_{ON,D}$	Dynamic Specific ON-Resistance
$R_{ON,S}$	Static Specific ON-Resistance
$R_{ON,SP}$	Specific on-resistance
S.S	Subthreshold Slope
σ	Capture Cross Section
T	Temperature
t_{BD}	Breakdown Time
τ_e	Electron Emission Time Constants
V_{DS}	Drain to Source Voltage
V_G	Gate Voltage
V_{GS}	Gate to Source Voltage

V_{ON}	Onset Voltage
V_{th}	Threshold Voltage
v_{th}	Thermal Velocity of Electrons
χ_{ox}	Electron Affinity of Oxide

List of Abbreviations and Acronyms

Term	Initial Components of the Terms
AC	Alternating Current
Al	Aluminum
AlN	Aluminum Nitride
AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
AlGaN	Aluminum Gallium Nitride
Al_2O_3	Aluminum oxide
Ar	Argon
Au	Gold
BCl_3	Boron Trichloride
C	Carbon
CeO_2	Cerium Oxide
CF_4	Tetrafluoromethane
CMOS	Complementary Metal Oxide Semiconductor
CMU	Capacitance Measure Unit
CL	Core Level
Cl_2	Chlorine
C-V	Capacitance-Voltage
DC	Direct Current

DI water	Deionized Water
D-mode	Depletion Mode
E-beam	Electron-beam
E-mode	Enhancement Mode
FET	Field Effect Transistor
Ga	Gallium
GaAs	Gallium Arsenide
$GaCl_3$	Gallium Trichloride
GaN	Gallium Nitride
GNDU	Ground Unit
HCl	Hydrogen Chloride
HF	Hydrofluoric Acid
HfO_2	Hafnium Oxide
HEMT	High Electron Mobility Transistors
H_2O	Water
HPSMU	High Power Source/Measure Units
HRSMU	High Resolution Source/Measure Units
HVSMU	High Voltage Source/Measure Units
ICP	Inductive Coupled Plasma
LPCVD	Low pressure Chemical Vapor Deposition
MIS	Metal-Insulator-Semiconductor
N_2	Nitrogen

Ni	Nickle
NH_3	Ammonia
$(NH_4)_2S$	Ammonium sulfide
O_2	Oxygen
ODT	1-Octadecanethiol
PBTI	Positive Bias Threshold-voltage Instability
PECVD	Plasma Enhanced Chemical Vapor Deposition
RIE	Reactive Ion Etching
RF	Radio Frequency
RTA	Rapid Thermal Annealing
S	Sulphur
SAM	Self-Assembled Monolayer
Si	Silicon
SiO_2	Silicon Oxide
Si_3N_4	Silicon Nitride
TCAD	Technology Computer Aided Design
TDDB	Time Dependent Dielectric Breakdown
TaN	Tantalum Nitride
Ti	Titanium
TiN	Titanium Nitride
TMA	Trimethylaluminum
TiO_2	Titanium Oxide

2DEG	Two-Dimensional Electron Gas
XPS	X-ray Photoelectron Spectroscopy
Zr	Zirconium
ZrO_2	Zirconium Oxide

CHAPTER 1 Introduction

1.1 Background

The electronic and semiconductor industries have been dominated by silicon-based CMOS fabrication technology since the 60's of last century. However, for high power applications, the silicon-based devices are not suitable enough owing to the limitations of silicon-based materials on channel mobility, critical breakdown field, and operating temperatures [1]. With the development of power electronics, the replacement of silicon by an adequate material becomes necessary in the field of high-power applications.

The power-related material properties (Energy Gap, Breakdown electric field, Saturation velocity, Thermal conductivity and Mobility) of Si, GaAs, SiC and GaN have been summarized in Table 1.1. The AlGaAs/GaAs high electron mobility transistors (HEMTs) are considered as the first generation of III-V materials-based devices [2]. One important advantage is a high density of two-dimensional electron gas (2DEG) existed at the AlGaAs/GaAs heterojunction. However, the small critical breakdown caused by its narrow bandgap is not appropriate for high voltage applications. The large bandgap of SiC is attractive for high voltage applications, but the mediocre carrier mobility in SiC-based devices is a limiting factor for achieving low on-state resistance and fast switching speed. In contrast, the GaN-based devices are expected to be applied in high power systems owing to superior material properties of high critical breakdown field, high carrier mobility and high saturation velocity [3]. These outstanding material

properties enable the GaN-based devices to be applied in high voltage, large current density, and fast switching speed systems.

Table 1.1 Comparison of the power-related material properties of Si, GaAs, SiC and GaN [3]

Properties	**Si**	**GaAs**	**SiC**	**GaN**
Band Gap (eV)	1.12	1.43	3.26	3.39
Critical Field (MV/cm)	0.23	0.5	2.2	3.3
Electron Mobility ($cm^2/V•s$)	1400	600	950	1500
Saturation Velocity (10^7 cm^2/s)	1.0	1.0	2.0	2.5
Thermal Conductivity (W/cm•K)	1.5	0.5	3.8	1.3

In high power applications, the conventional GaN-based HEMT devices suffer from large gate leakage currents due to the Schottky-gate contacts. By replacing the Schottky-gate contact with a metal-insulator-semiconductor (MIS) structure, gate leakage currents can be suppressed significantly. For the application of GaN-based MIS-HEMTs in power electronics, one important challenge is the realization of low interface density between the GaN-based material and dielectrics. A high trap density at the gate dielectric/GaN interface and passivation/GaN interfaces would cause gate leakage currents, surface leakage currents, the degradation of sub-threshold characteristics and the degradation of dynamic resistance [4]. In order to reduce the interface state density, GaN surface treatments have been suggested as critical procedures prior to the dielectric deposition. Techniques such as acid clean [5], gas plasma [6], and sulfide-based passivation schemes [7] have been investigated to reduce the interface states density. Details of the above-mentioned treatment techniques will

be reviewed in Section 1.2.

In addition, the off-state breakdown and dynamic performances of the GaN-based MIS-HEMTs are also important for high power applications. Though a high gate breakdown voltage can be achieved using the MIS structure, the reliability issues induced by the passivation layer under high electric field and dynamic switching ambient are still a major concern. Most of the conventional passivation materials on MIS-HEMTs are SiO_2 or SiN_x with relatively low relative permittivity ($\varepsilon_r < 7$), wide bandgap ($E_G > 5$ eV), and high critical breakdown field ($E_f \sim 20$ MV/cm) [8, 9]. Moreover, the high-*k* materials deposited by atomic layer deposition (ALD) also show great potential and advantages as a choice for the passivation layer [10]. Details of the abovementioned passivation layers will be reviewed in Section 1.3.

Furthermore, the development of normally-off GaN-based devices with good on-state conductivity is another important issue for high power applications. Owing to the polarization effect between AlGaN and GaN, a sheet of 2DEG exists at the AlGaN/GaN interface. Therefore, the AlGaN/GaN HEMTs or MIS-HEMTs exhibit normally-on operation if no special gate design is carried out. In power circuit applications, the normally-off GaN-based devices are preferred for safety consideration. Several approaches have been explored to realize the normally-off operation of devices, such as AlGaN barrier recess [11], p-type GaN cap layer [12], fluorinated-gate structure [13] and oxide charge engineering [14]. Details of the abovementioned techniques to realize the normally-off operations will be reviewed in Section 1.4.

1.2 Overview of dielectrics/GaN interface treatments

For the GaN-based devices with MIS gate structure, the gate dielectric material is suggested to exhibit wideband offsets to GaN to form a barrier for both electrons and holes. Some feasible insulators, such as SiO_2 [15], Si_3N_4 [16], AlN [17], Al_2O_3 [18], and HfO_2 [19] have been considered for MIS gate structures. Among these materials, the Al_2O_3 with a large conduction and valence band offsets (2.05 eV and 1.08 respectively) [20] to GaN and a high relative permittivity (~9) [21], hence it was chosen as the gate dielectric in this study. However, a high interface trap density of ~$1x10^{13}$ $cm^{-2}eV^{-1}$ at the Al_2O_3/GaN interface has been reported [22]. This poor interface quality has been associated with the native gallium oxide and dangling bonds on the GaN surface [4], resulting in large leakage currents and a threshold voltage instability. In order to reduce the trap density at the Al_2O_3/GaN interface, the treatments on the GaN surface have been proposed as critical procedures to remove native oxide on GaN or to passivate the states prior to the Al_2O_3 deposition.

The most conventional and economical treatment method is the acid-based surface cleaning for eliminating the native oxide or contaminants on the GaN surface. HCl [5] and HF [23] solutions are commonly used to remove the native oxide and metal ions, but the exposed GaN surface suffers from re-oxidation before the gate dielectrics deposition. In addition, the piranha solution (H_2O_2: H_2SO_4 = 1:5) is capable of removing the carbon contaminations and create a smooth GaN surface [23]. However, the suppression of the trap density at the Al_2O_3/GaN interface is not significant using this technique.

Based on acid-based treatment techniques, the sulfide-based passivation schemes, such as aqueous $(NH_4)_2S$ solution, was proposed to protect the GaN surface from immediate re-oxidation by forming Ga-S bonds [7]. However, metal contamination of the $(NH_4)_2S$ solution and the limited stability of the $(NH_4)_2S$ passivation during the fabrication processes [24] are two limitations, which might be detrimental to the performances of devices. A recent study [25] reported that 1-Octadecanethiol (ODT) solution could protect the GaAs surface from oxidation. In addition, the GaAs surface passivated by ODT self-assembled monolayer (SAM) exhibits an improved passivation stability in an air ambient [26].

In addition, studies have also reported that the oxidation of GaN surface is able to fill up the Ga dangling bonds, and form a high quality Ga-oxide layer on the GaN surface [6]. Compared with the thermal oxidation technique with low uniform properties, the low power O_2 plasma treatment [27] is considered as a more effective method to passivate the Ga dangling bonds and to remove possible carbon contamination on the GaN surface. Moreover, a recent study reported an effective but more complicated technique to reduce the interface state. This technique applies an in-situ remote $NH_3/Ar/N_2$ plasma to remove the native surface oxide and to passivate the GaN surface using N atoms with minimum surface damage [28].

1.3 Overview of the passivation layer on GaN-based devices

The low-pressure chemical vapor deposition (LPCVD) of SiN_x has been widely applied as the gate dielectric or passivation layer of the GaN-based MIS-HEMTs [9]. LPCVD-Si_3N_4 is considered as a promising gate dielectric for AlGaN/GaN MIS-HEMTs, owing to the high quality film and the low trap density at the LPCVD-Si_3N_4/(Al)GaN interface. The devices with LPCVD-Si_3N_4 dielectric exhibit decent properties such as suppressed leakage currents, long time-dependent dielectric breakdown lifetime, high breakdown voltage, and low current collapse effect [29, 30]. The high temperature and the low deposition rate make LPCVD-Si_3N_4 not optimal to be employed as the passivation layer. This is because the degradation of ohmic contact electrodes may occur during the high temperature (> 650 ℃) deposition process. A possible solution for achieving thick LPCVD-Si_3N_4 passivation is to grow at a much higher temperature (780 ℃) prior to the ohmic contact process [20]. However, cracks on the LPCVD-SiN_x passivation layer is difficult to avoid after the ohmic alloying.

The plasma enhanced chemical vapor deposition (PECVD) of Si_3N_4 or SiO_2 grown with a faster deposition rate at a lower temperature of ~350 ℃ has long been a common passivation layer for the GaN-based MIS-HEMTs [31]. However, low breakdown voltage, large leakage currents, and serious current collapse effect are commonly observed on these devices [31-33]. This is because the exposure of (Al)GaN surface to the aggressive plasma in the PECVD process may cause the degradation of (Al)GaN surface, surface trap density and surface leakage currents [34]. The plasma enhanced atomic layer deposition (PEALD) is also attractive for the Si_3N_4 deposition due to the

high film quality and precise thickness control ability at low temperatures. A recent study [35] demonstrated robust AlGaN/GaN MIS-HEMTs with a suppressed current collapse by using the PEALD-Si_3N_4 passivation layer. Note that, the deposition rate of PEALD-Si_3N_4 is a quite low value of 0.01 nm/cycle, which is not suitable for deposing thick passivation in high voltage devices fabrication.

The high-*k* materials deposited by atomic layer deposition (ALD) have been commonly researched as the gate dielectric in GaN-based MIS-HEMTs, for example, Al_2O_3 (relative permittivity ε_r = ~9) [36], HfO_2 (ε_r = ~20) [27], ZrO_2 (ε_r = ~30) [37], and TiO_2 (εr = ~55) [38]. Those dielectrics possessed excellent characteristics, such as free of plasma-induced damage, high film qualities, and lower deposition temperature. Compared with Si_3N_4 or SiO_2 deposited under plasma or high temperature ambient, the ALD high-*k* materials deposited with a rate of 0.1 nm/cycle at a low temperature of 300 ℃ also show great advantages as a choice for the GaN-based MIS-HEMTs passivation layer. An experimental study [39] demonstrated that high off-state breakdown AlGaN/GaN MIS-HEMTs is achieved by using an ALD-Al_2O_3/LPCVD-Si_3N_4 bilayer passivation structure. In addition, a simulation analysis [10] indicated that applying high-*k* passivation is capable of improving the breakdown voltage. Note that, the effects of the high-*k* passivation layer on the high voltage properties of GaN-based devices have not been fully discovered at present.

1.4 Overview of normally-off techniques for AlGaN/GaN HEMTs

Due to the polarization and piezoelectric effects at the AlGaN/GaN heterojunction, the fabricated HEMTs exhibit the normally-on operation if without special processes on the gate structure. In power circuit applications, the normally-off GaN-based devices are preferred for safety consideration. Several approaches have been explored to realize normally-off operations, such as gate recess [11, 41], p-type GaN cap layer [12], fluorinated-gate [13], and oxide charge engineering [14].

The gate-recess structure is formed by thinning the AlGaN barrier layer at the gate region (as shown in Fig. 1.1). The 2DEG density at the AlGaN/GaN interface can be depleted by recessing the AlGaN barrier, because the piezoelectric effect is reduced with a thinner AlGaN layer [41]. The devices exhibit the normally-off operations when the 2DEG is eliminated without a gate bias. With forward gate biases, electrons are formed at the gate dielectric/GaN or AlGaN/GaN interface to connecting source and drain. The devices combining fully recessed gate with high-quality gate dielectric techniques [42] demonstrate the normally-off operation and good V_{th} stability, but the current density is relatively low owing to the uncontrollable damages on the 2DEG channel.

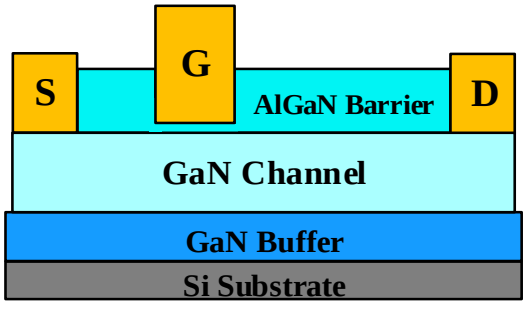

Fig. 1.1 Cross-sectional schematics of the gate recess structure

Fig. 1.2 demonstrates the schematic diagram of the devices with a p-GaN cap layer structure. The addition of the p-GaN cap above the AlGaN barrier is capable of depleting the 2DEG channel, thus creates a normally-off operation [43]. The p-type GaN normally-off devices [44] exhibit good V_{th} stability and low on-state resistance. However, the relative low V_{th} and the low gate breakdown voltage are two significant imperfections of the P-GaN HEMT devices. Moreover, the difficulty of dopant activation is another important issue for the p-GaN cap structure.

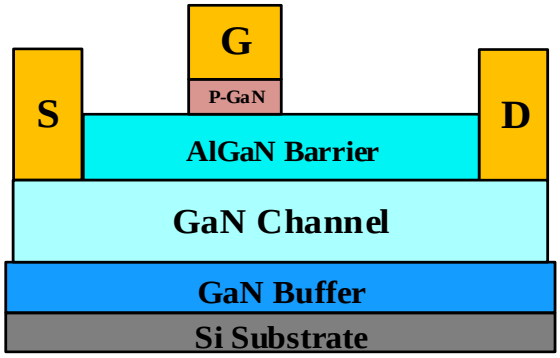

Fig. 1.2 Cross-sectional schematics of the p-GaN gate structure

Fig. 1.3 demonstrates the schematic diagram of the HEMT devices with a fluorinated-gate structure. This technique realizes the normally-off operation of devices by implanting fluorine ions into the AlGaN barrier layer [45] or the gate dielectric layer [13]. These fluorine ions act as negative fixed charges in the AlGaN layer or in the gate dielectric to deplete the 2DEG beneath. The AlGaN/GaN MIS-HEMTs combining partially recessed gate with fluorinated gate dielectric structure [46] demonstrate a very high V_{th}, however, the devices lack enough evidence on the thermal stability.

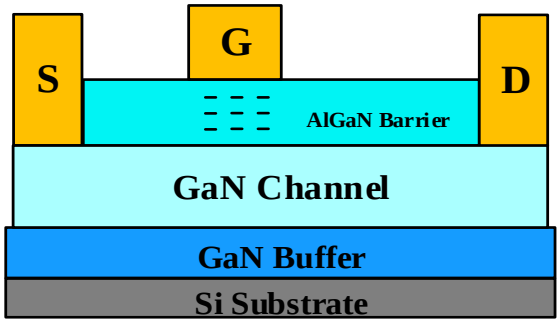

Fig. 1.3 Cross-sectional schematics of the fluorinated-gate structure

The GaN-based MIS-HEMTs with a charge storage gate structure (as shown in Fig. 1.4) have been proposed to forwardly shift the V_{th} for achieving the normally-off operation without a large current degradation. A simulation analysis [47] indicated that the negative charges in a floating gate or an oxide layer are capable of depleting the 2DEG beneath the gate region, resulting in a normally-off operation. In addition, some experimental studies reported that the normally-off MIS-HEMTs could be realized by using charge storage structure, such as the TaN floating gate [48], the HfO_2 charge storage layer [49], and the Al_2O_3 charge storage layer [50]. Furthermore, normally-off MIS-HEMTs with a high V_{th} and a high drain current density have been demonstrated by using the combination of ferroelectric and charge storage layers [51]. Even though the reported MIS-HEMTs with charge trapping structure achieved outstanding normally-off device properties, the complex gate structures and the limited charge storage capacity are still important issues for the fabrication and application of high power devices

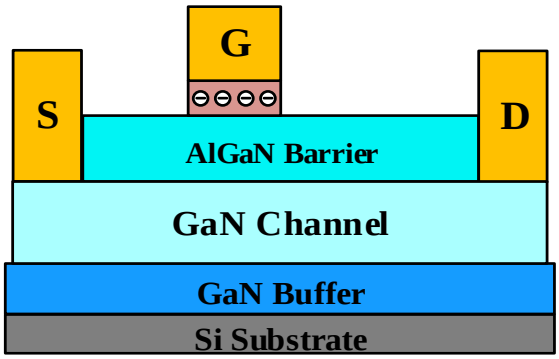

Fig. 1.4 Cross-sectional schematics of the charge storage structure

1.5 Aims and Objectives

This research aims to fabricate the normally-off AlGaN/GaN MIS-HEMTs with high breakdown voltage and low on-state resistance. In order to achieve the aims of the thesis, the following six objectives will be realized in sequence,

1. To deposit Al_2O_3 as the gate dielectric of GaN-based devices and to fabricate AlGaN/GaN MIS-capacitors for investigating the states at the Al_2O_3/GaN interface, including the density of states, the energy level location of the states.
2. To investigate the effect of gate dielectric/GaN interface states on the C-V behavior of the MIS-capacitors and to understand how the interface states responding to the gate bias.
3. To reduce the Al_2O_3/GaN interface states density by using GaN surface pre-treatment techniques, and to fabricate AlGaN/GaN MIS-HEMTs with stable DC I-V characteristics.
4. To realize high voltage (over 1000 V) AlGaN/GaN MIS-HEMTs with low leakage currents and high breakdown voltage, and to suppress the current collapse effect of AlGaN/GaN MIS-HEMTs.
5. To deposit high-*k* materials as the passivation layer of AlGaN/GaN MIS-HEMTs, and to investigate the effect of high-*k* dielectrics on the high voltage performances of the devices.
6. To realize the normally-off AlGaN/GaN MIS-HEMTs with high breakdown voltage and good on-state conductivity.

1.6 Thesis organization

The thesis includes six chapters. Chapter 1 is the introduction of the thesis. Chapter 2 introduces the methodologies and operating principles of the simulation, fabrication, and characterization used in the thesis. Chapters 3~5 demonstrate the major work of the thesis.

In Chapter 3, in order to improve the Al_2O_3/GaN interface quality, a low-cost and effective method of the ODT treatment is proposed. Before the device fabrication, the TCAD simulation was firstly carried out to understand the C–V behavior of AlGaN/GaN MIS-capacitors. For the fabricated devices, comparisons have been made among without any treatment and with the HCl, oxygen plasma, and ODT treatments prior to the gate dielectric deposition. The chemical composition on the GaN surface with different treatments and the electrical characteristics of MIS devices with ALD-Al_2O_3 gate dielectric has been demonstrated. This work is important for achieving reliable AlGaN/GaN MIS-HEMTs with suppressed leakage currents and satisfied subthreshold characteristics.

In Chapter 4, high-*k* dielectrics were employed as the passivation layer to improve the breakdown voltage and dynamic performances of AlGaN/GaN MIS-HEMTs. Before the device fabrication, a TCAD simulation of breakdown voltage and electric field profiles in MIS-HEMTs as functions of the device structures was performed. After that, the AlGaN/GaN MIS-HEMTs with different passivation layers (with/without high-*k* dielectric interlayer) have been fabricated. The high-*k* dielectrics, Al_2O_3 and ZrO_2 as the interlayer between GaN cap and PECVD-SiN_x passivation are considered.

Reduced dynamic on-resistance and improved breakdown voltage are simultaneously exhibited on the MIS-HEMTs with high-*k* dielectrics interlayer, indicating an enormous potential of the proposed high voltage devices structure.

In Chapter 5, firstly, the normally-off AlGaN/GaN MIS-HEMTs are realized by using a fully recessed gate structure. However, the low current density and large on-states resistance exhibited on the devices are not suitable for high power applications. Afterward, the deposition of the ZrO_x charge trapping layer on the partially recessed AlGaN in conjunction with the Al_2O_3 gate dielectric was developed. The employing of the AlGaN partially recess technique enables a forward shift on the V_{th} without damaging the AlGaN/GaN interface. The deployment of the ZrO_x trap charging layer is capable of depleting the 2DEG beneath to realize the devices with E-mode operation. The fabricated MIS-HEMTs exhibits highly desired performance, including a positive V_{th}, a high current density, a high I_{ON}/I_{OFF} current ratio, a high off-state breakdown voltage, and a small current collapse effect.

In Chapter 6, the thesis is summarized with recommendations on future works.

1.7 Published works

[1] Y. Cai, W. Liu, M. Cui, R. Sun, Y. C. Liang, H. Wen , L. Yang, S. N. Supardan, I. Z. Mitrovic, S. Taylor, P. R. Chalker, and C. Zhao. "Effect of Surface Treatment on Electrical Properties of GaN Metal Insulator-Semiconductor Devices with Al_2O_3 Gate Dielectric," *Japanese Journal of Applied Physics*, vol. 59, no. 4, pp. 041001, 2020.

[2] Y. Cai, Y. Wang, Y. Liang, Y. Zhang, W. Liu, H. Wen, I Z. Mitrovic, and C. Zhao. "Effect of High-*k* Passivation Layer on High Voltage Properties of GaN Metal-Insulator-Semiconductor Devices," *IEEE Access*, vol 8, no. 1, pp. 95642-95649, 2020.

[3] Y. Cai, Y. Zhang, Y. Liang, W. Liu, H. Wen, and C. Zhao. "Low On-state Resistance Normally-OFF AlGaN GaN MIS HEMTs with ZrO_x Charge Trapping Layer for High Power Applications," *IEEE Electron Device Letters*, under review.

[4] M. Cui, Q. Bu, Y. Cai, R. Sun, W. Liu, H. Wen, S. Lam, Y. C. Liang, I. Z. Mitrovic, and S. Taylor, "Monolithic integration design of GaN-based power chip including gate driver for high-temperature DC–DC converters," *Japanese Journal of Applied Physics*, vol. 58, no. 5, pp. 056505, 2019.

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CHAPTER 2 Device Simulation, fabrication and characterization techniques

The study in this thesis consists of the simulation, fabrication, and characterization of AlGaN/GaN MIS-capacitors and MIS-HEMTs. This chapter begins with the introduction of the simulation of GaN-based devices. The simulation analysis is a powerful tool to understand the inherent physical properties and to provide guidelines for the design of devices. In chapter 3, the C-V characteristics of oxide/AlGaN/GaN MIS-capacitors were investigated by using the Sentaurus TCAD tools, and the gate dielectric/AlGaN interface properties were focused on. Moreover, in chapter 4, the device simulations were important for the selection of the passivation layer in the GaN-based high voltage devices. The simulation results provide a clear explanation of how the permittivity of the passivation layer affecting the breakdown voltage of AlGaN/GaN MIS-HEMTs. A detailed introduction of the Sentaurus device simulation tool is discussed in Section 2.1. In Sections 2.2, the fabrication process of the fabricated devices in Chapters 3, 4, and 5 are summarized in flowcharts, and all of the facilities used in the fabrication process are provided. Furthermore, the detailed operating principles of the characterization methodologies for the AlGaN/GaN devices are described in Section 2.3.

2.1 Process of TCAD simulation analysis

The device simulations were implemented in 2-D by Synopsys Sentaurus TCAD tools [1-3]. The TCAD simulation analysis is capable of visualizing the physical properties inside of the devices and assisting in the design of high voltage HEMTs in this study. The simulations are organized in three Sentaurus Workbench projects, which include Sentaurus structural editor unit, Sentaurus device unit, and Sentaurus visual unit. The structural editor unit was used to create the device structure. The Sentaurus device unit was used to simulate the electrical and physical characteristics of devices. The Sentaurus visual unit was used to plot the electrical and physical characteristics of devices.

The first step of the simulation is the drawing of the devices' structure and meshes by coding the .cmd file in the Sentaurus structural editor unit. The .cmd file started from defining the dimension, location, and parameter of each component of devices. Such as dielectrics, GaN buffer, AlGaN barrier, metals, the doping concentration of semiconductor, et al. Note that, in the 2D TCAD analysis, the cross section of the device was considered as the normalized structure for representing the real devices. The mesh layout was then drawn inside of each component of devices and at the interfaces between each component. The density of the mesh decides the calculation amount as well as the accuracy, which is determined by the assigned conditions in the structural editor. Moreover, the simulation could be convergence failed if the mesh was unsuitable for the structure. Therefore, a proper design on the mesh density is important to obtain reliable results. Fine meshes are commonly required at the electric field regions, such

as the electrode edges, the barrier layer surface, and the 2DEG Channel. In contrast, coarse meshes are acceptable on the regions with slow changes, such as GaN buffer. Fig. 2.1 illustrates the layout of the devices with meshes drawn.

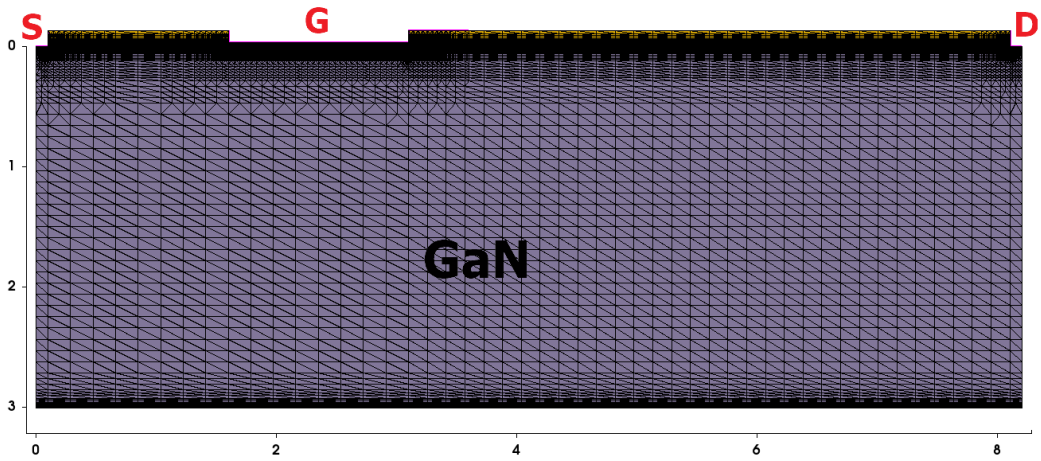

Fig. 2.1 An example of the structure and meshes used in the AlGaN/GaN MIS-HEMTs simulation

After completed the structure design in Sentaurus structural editor unit, the generated structure, mesh, and doping information are stored in a TDR file. This TDR file was then passed to the Sentaurus Device unit, which was used to compute the device characteristics. Here, the TDR file, physical models, and parameter files were combined in the simulation with an appropriate mathematical configuration. The device characteristics were calculated as similar sequences as the corresponding electrical measurements.

2.2 Fabrication process and Facilities used for AlGaN/GaN MIS-devices

The fabrication procedure for AlGaN/GaN MIS devices in this thesis includes the organic & inorganic cleaning, photolithography, inductive coupled plasma (ICP) etching or AlGaN & GaN dry etching, electron-beam (e-beam) evaporator for metals evaporation, rapid thermal annealing (RTA) for ohmic contact formation, atomic layer deposition (ALD) for Al_2O_3, ZrO_2 and ZrO_x dielectrics deposition, oxides wet etching; oxygen gas plasma reported in Chapter 3; plasma-enhanced chemical vapor deposition (PECVD) for SiN_x deposition reported in Chapter 4 and 5; reactive ion etching (RIE) for SiN_x dry etching reported in Chapter 4 and 5, and O_2 plasma plus HCl based digital etching for AlGaN wet etching reported in Chapter 5.

The fabrication process of MIS-capacitors and normally-on MIS-HEMTs reported in Chapter 3 is plotted as a flowchart in Fig. 2.2. The fabrication process of high voltage normally-on MIS-HEMTs reported in Chapter 4 is plotted as a flowchart in Fig. 2.3. The fabrication process of low-resistance normally-off MIS-HEMTs reported in Chapter 5 is plotted as a flowchart in Fig. 2.4.

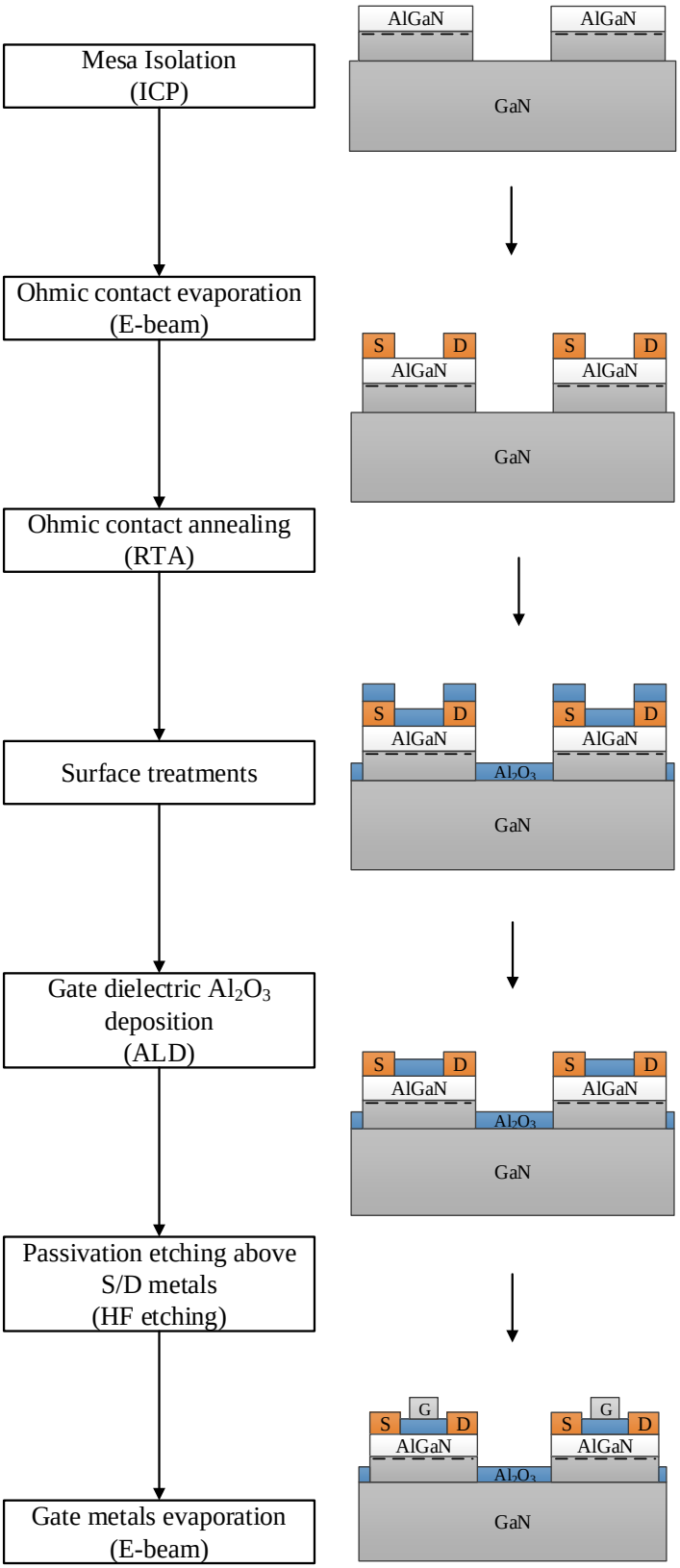

Fig. 2.2 The fabrication procedure of GaN-based MIS-capacitors and normally-on MIS-HEMTs reported in Chapter 3

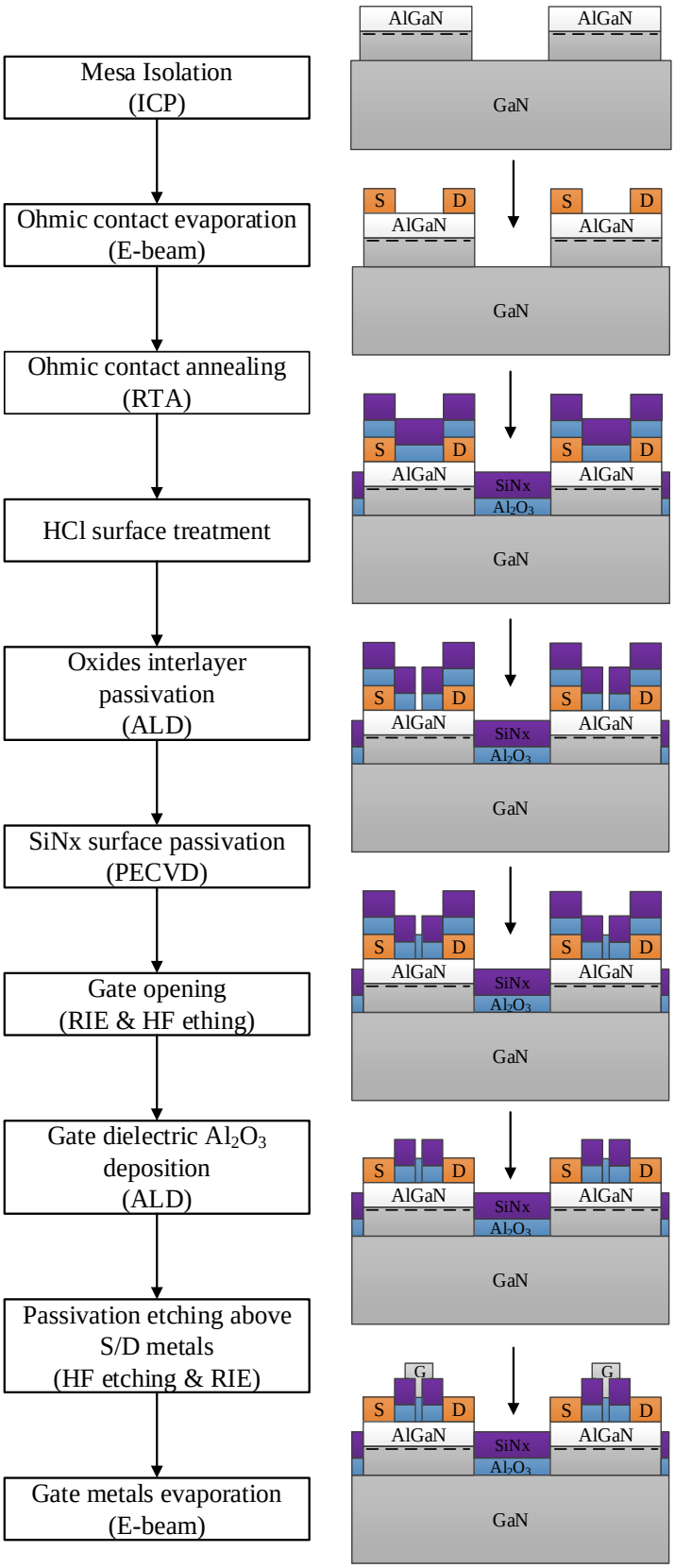

Fig. 2.3 The fabrication procedure of GaN-based Normally-on MIS-HEMTs reported in Chapter 4

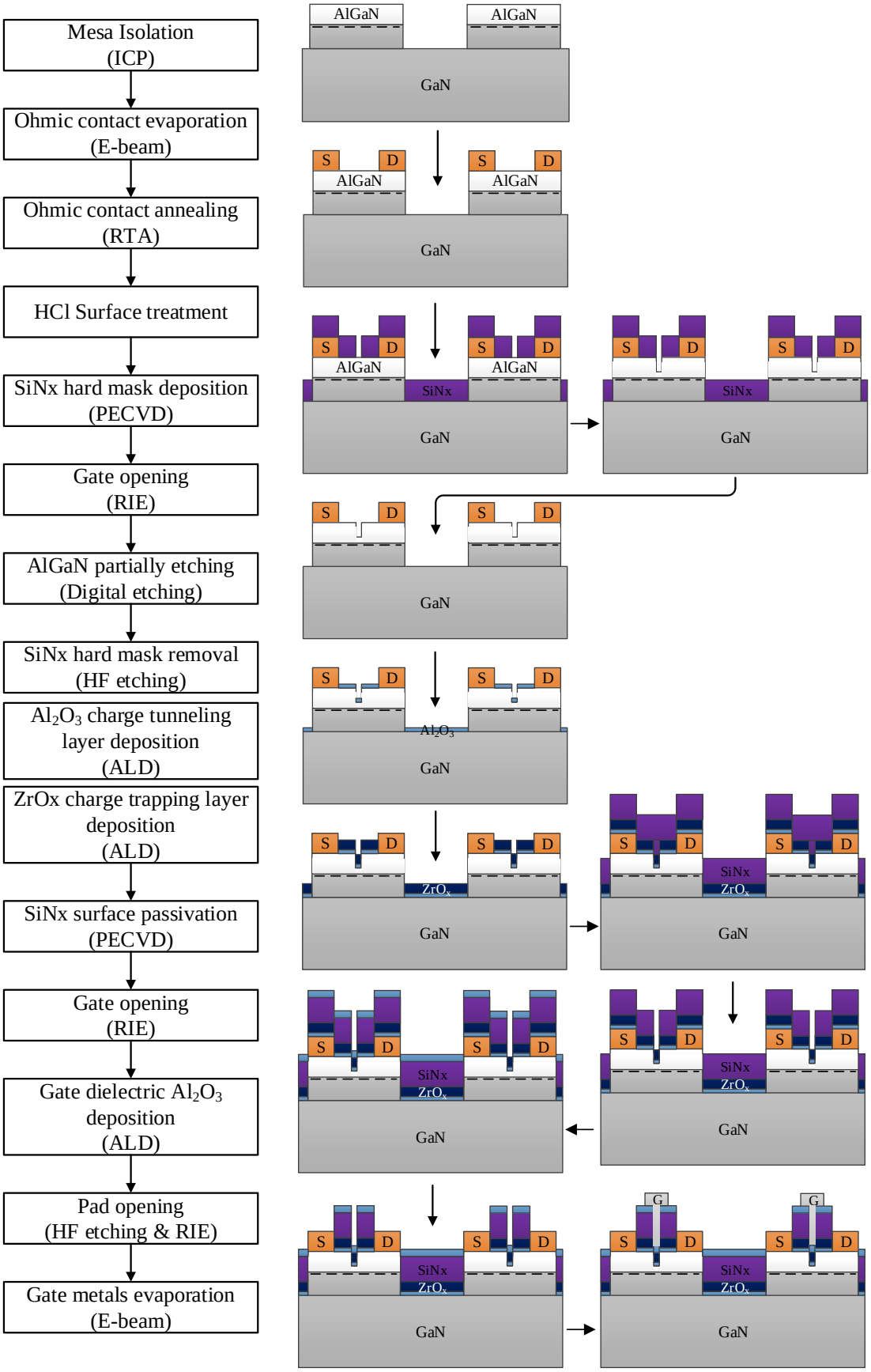

Fig. 2.4 The fabrication procedure of GaN-based normally-off MIS-HEMTs reported in Chapter 5

The mesa isolation in Chapters 3, 4, and 5 was carried out by using ICP etching to define the active region of the devices. The ICP etching combines the physical and chemical reaction on the GaN-based surface, which is a commonly used dry etching technique. The radio frequency (RF) power source in the ICP system is able to generate a strong electromagnetic field that dissociates the gas molecules into electrons, ions, and chemically-active radicals. As ions do not have high enough mobility to keep up with the changing of the RF field, fewer ions than electrons are collected at the plates [4]. Therefore, the samples placed on the plate receive continuous bombardment from the ions. Meanwhile, the power source in the ICP system controlled the concentration of radicals and ions and the ion bombardment energy to provide good selectivity and anisotropy. BCl_3 and Cl_2 gases were used as effective etchants for AlGaN and GaN-based on the formation of volatile $GaCl_3$ after the ICP etching [5].

The ohmic contact on the GaN-based devices is needed for realizing a low resistance between the 2DEG channel and the source/drain electrodes. The AlGaN barrier has a large band-gap in the HEMT heterojunction structure, and the band discontinuities exist when the AlGaN is associated with the GaN. The high Schottky barrier at the metal-AlGaN interface is a limiting factor in achieving low contact resistance. The formation of ohmic contact was commonly implemented by depositing stacks of metal with proper annealing afterward. The annealing process is capable of activating the reaction between the metal and the GaN-based material, alternating the surface state to form ohmic contacts. The bottom metal Ti can react with the AlGaN to form TiN under appropriate high temperature. Meanwhile, N vacancies would be

generated at the AlGaN layer after the alloy reaction. Note that, the formed TiN and N vacancies play an important role in the ohmic contact formation. The N vacancies behave like the n-type doping ions that create a tunneling junction from metal to the 2DEG channel. The most commonly used pattern of the metals in ohmic contact was the Ti/Al/Ni/Au, however, Au-containing schemes increase the cost of device products. In addition, a good morphology of the contact surface and a well-defined edge are also important for the high-power performance of GaN-based devices. In this thesis, the Au-free ohmic contact scheme was realized by evaporating Ti/Al/Ni/TiN metals stack and annealed in N_2 ambient by using rapid thermal annealing (RTA).

The transmission line model was used to measure the contact resistance for planar ohmic contacts. The basic pattern contains two contacts at the ends, and the voltage was measured between one of the large contacts and each of the small contact strips. The common testing scheme is shown in Fig. 2.5.

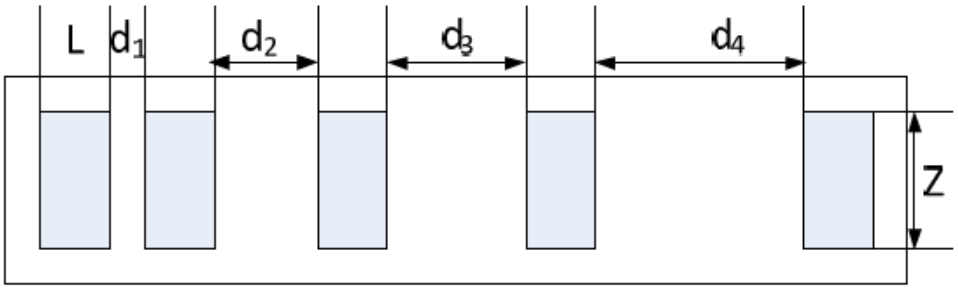

Fig. 2.5 The Schematic transmission line model testing circuits

where L is the length of the pad, Z is the width, and d_i is the pad spacing. The total resistance (R_T) between any adjacent two contacts could be plotted as a function of the pad spacing. It was assumed that the sheet resistance (R_S) under contact and outside the contact are identical. The contact resistance (R_C) can be estimated by setting the pad

spacing equals to 0. When the TLM pattern includes electrically long contacts which have d >> L, and using different d and R_T values, R_C can be extracted from the relationship in Eq. (2.1).

$$\frac{R_T}{Z} = 2R_C + \frac{R_S d}{Z} + \frac{2R_S L}{Z} \approx 2R_C + \frac{R_S d}{Z} \quad (2.1)$$

The R_C in this study was evaluated by measuring the values of total resistance R_{Ti} at the various values of pad spacing d_i. Here, R_C can be expressed as

$$R_C = \frac{R_{Ti}}{2Z} - \frac{R_S d_i}{Z} \quad (2.2)$$

by setting the pad spacing d_i equals to 0 in the function of R_{Ti} versus d_i, the contact resistance R_C can be calculated as Eq. (2.3).

$$R_C = \frac{R_{T\,(d=0)}}{2Z}\ (\Omega \cdot mm) \quad (2.3)$$

However, this is an approximation calculation of the contact resistance because the layer resistances under the contact and outside the contact are the same. For most cases of the metal-semiconductor contact, using Eq. (2.3) is a simple way for giving out the contact resistance.

The digital etching in Chapters 5 was carried out to slowly recess the GaN cap and the AlGaN barrier layer beneath the gate area. In each digital etching cycle, the process was carried out as a low power O_2 plasma oxidation followed by an HCl-based oxide removal. In specific, a 100 W O_2 plasma generated by RIE was used to oxidize the GaN and the AlGaN to the GaO_x and the AlO_x, and then the 10% HCl solution was used to recess the oxides. The low damage digital etching with an etching rate of 0.4 nm/cycle was verified by Atomic Force Microscopy (AFM). This technique is beneficial to control the etching depth precisely as well as keep a uniform surface roughness. The

schematic of the digital etching process is illustrated in Fig. 2.6.

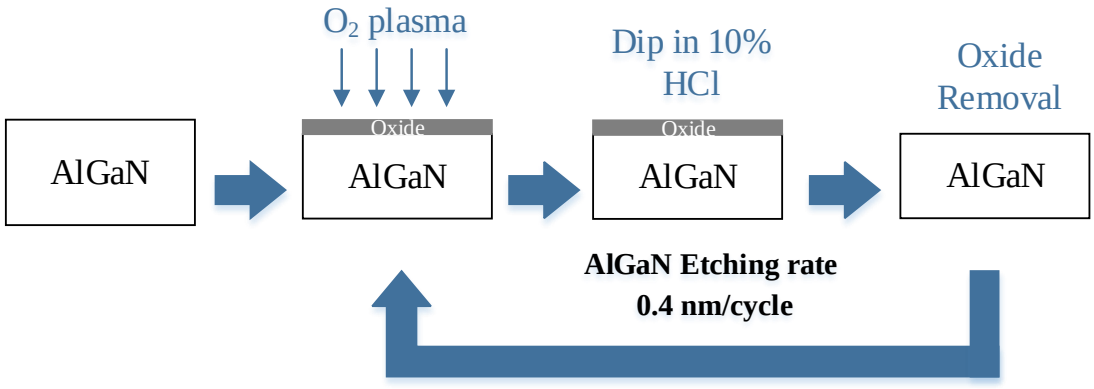

Fig. 2.6 The schematic of the digital etching process

The atomic layer deposition (ALD) in chapters 3, 4, and 5 is a technique that deposits monolayer-level films with an excellent uniform and conformal structure. The ALD process is considered as a binary reaction sequence where a surface exchange reaction between the metal-containing precursor and the oxidant source occurs to form a thin film. In this thesis, ALD is used to deposit the Al_2O_3 gate dielectric, the Al_2O_3 passivation layer, the ZrO_2 passivation layer, and the ZrO_x charge tarping layer. The deposition of Al_2O_3 film in this thesis uses H_2O and Trimethylaluminum (TMA) precursors as the source of O and Al atoms for Al_2O_3 formation. The deposition of ZrO_2 and ZrO_x in this thesis uses H_2O and Tetrakis (ethylmethylamino) zirconium precursors as the source of O and Zr atoms for ZrO_2 or ZrO_x formation.

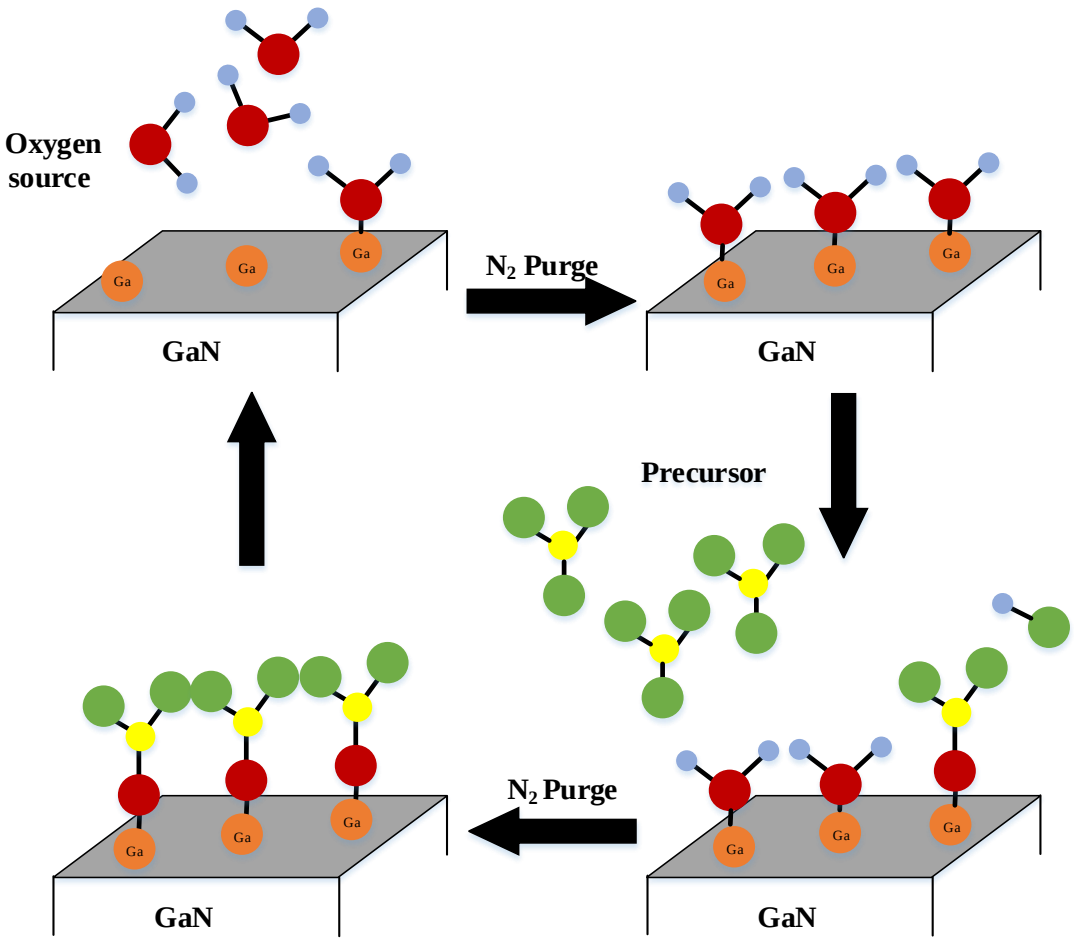

Fig. 2.7 The schematic of the ALD deposition process

The schematic of the ALD deposition process is illustrated in Fig. 2.7. The process started with the oxidant source pulse, here, the oxidant source reacts with the substrate surface to form metal-oxide bonds (Fig. 2.7 (a)). After purging N_2 to evacuate the excessive oxidant source in the chamber (Fig. 2.7 (b)), the metal-containing precursor is introduced to react with the oxides on the substrate surface to create metal-oxide-metal bridges (Fig. 2.7 (c)). After that, the unreacted metal-containing precursor and organic gas are evacuated from the chamber with N_2 purge (Fig. 2.7 (d)). In this study, the deposition rate of Al_2O_3, ZrO_2, and ZrO_x is 0.11 nm/cycle, 0.11 nm/cycle, and 0.1

nm/cycle, respectively, which was evaluated from the best fit from spectroscopic ellipsometry measurements.

The Plasma enhanced chemical vapor deposition (PECVD) used in chapters 4 and 5 is a thin film deposition technique. One important advantage is its capability of operating at low temperatures with a faster deposition rate. In this thesis, the PECVD system was used to deposit the SiN_x passivation layer with SiH_4 and NH_3 as the reactant gases. The RF-power in the PECVD system generates plasma to enhance the energy required to initiate the deposition. The overall reaction of the SiN_x deposition is shown in Eq. (2.4),

$$SiH_4+NH_3 \rightarrow SiN_x+H_2+N_2 \qquad (2.4)$$

where H_2 and N_2 are the by-products of the reactions which can be easily pumped away from the chamber. The SiN_x deposition rate is approximately 65 nm/min at a chuck temperature of 350 ℃, which was evaluated from spectroscopic ellipsometry measurements.

The etching of SiN_x was carried out by using RIE with CF_4 and O_2 as the reactant gas. In the RIE system with an RF power supply, the CF_4 will be dissociated into C and F radicals, and the O_2 plasma is generated for the carbon removal. The F radicals tend to react with SiN_x and form gaseous SiF_4 and N_2. The total reaction is shown in Eq. (2.5). The PECVD-SiN_x etching speed is evaluated as 140 nm/min.

$$F^-+SiN_x \rightarrow SiF_4+N_2 \qquad (2.5)$$

2.3 Characterization methodologies for AlGaN/GaN MIS-devices

To understand the performance and the underlying physics of the fabricated devices, characterizations on the GaN surface bonding and electrical properties were carried out. These characterizations were implemented by using X-ray photoelectron spectroscopy (XPS), power device analyzer Keysight B1505A and semiconductor analyzer Keysight B1500A. The electrical properties of the GaN-based MIS-device were characterized using the I_D-V_{DS} measurement, the I_D-V_{GS} measurement, the I_G-V_{GS} measurement, the capacitance-voltage (C-V) measurement, the time dependent dielectric breakdown (TDDB) measurement, the positive bias threshold-voltage instability (PBTI) measurement, the current collapse measurement, and the off-state breakdown voltage measurement.

The I_D-V_{DS} measurement, I_D-V_{GS} measurement, and I_G-V_{GS} measurement were carried out using two high-resolution source/measure units (HRSMU) and one ground unit (GNDU) on the power device analyzer Keysight B1505A. The MIS-transistors were probed by a probe station system, and the measurement circuit is illustrated as Fig. 2.8. The source of MIS-transistor connects to the GNDU, the gate and the drain connects to the two HRSMUs. For the I_D-V_{DS} measurement, the gate signal was step varied from a voltage less than the V_{th} to a positive gate bias, and the step of V_G variation was usually larger than 1 V. The drain signal was swept from 0 to a positive bias at each constant V_G, and the sweeping resolution was set as 0.25 V. For the I_D-V_{GS} measurement, the drain signal was fixed at a constant positive bias to form a voltage potential on the drain. The gate signal was swept from a voltage less than the V_{th} to a

positive gate bias. The maximum gate bias was the same as that in the I_D-V_{DS} measurement, and the sweeping resolution was set as a low value of 20 mV. For the I_G-V_{GS} measurement, the drain was floating. The gate signal was swept from a negative voltage to the maximum tolerable gate bias. The compliance current of HRSMU was set a 1 mA to protect the measurement system.

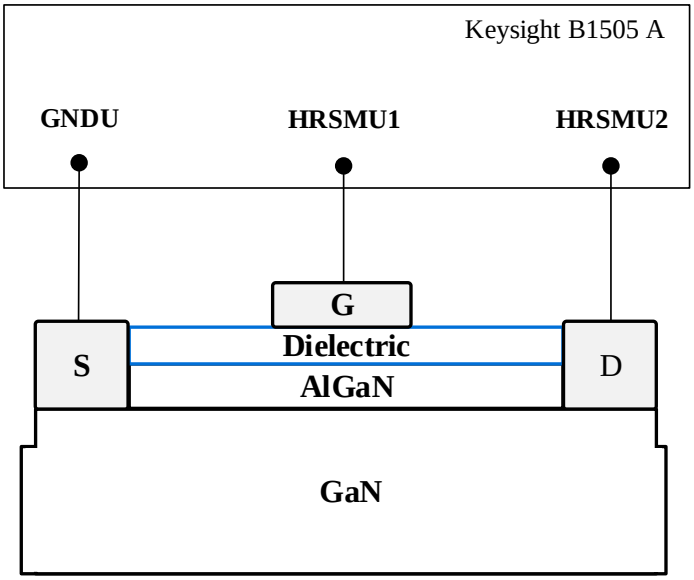

Fig. 2.8 The measurement circuit for the I_D-V_{DS} measurement, I_D-V_{GS} measurement and I_G-V_{GS} measurement

The CV measurement was carried out using a positive capacitance measure unit (CMU+) and a negative capacitance measure unit (CMU-) on the semiconductor analyzer Keysight B1500A. The MIS-capacitors or MIS-transistors were probed by a probe station, and the measurement circuit is illustrated as Fig. 2.9. The CMU+ was connected to the gate, the CMU- was connected to the source, and the drain was floating. The DC gate signal was swept from a voltage less than the V_{th} to a positive gate bias, and the AC gate signal was fixed as 200 mV. The measurement frequency was varied

from 1 kHz to 2 MHz, and the measurement temperature was set as 25 ℃, 50 ℃, 75 ℃, 100 ℃ and 125 ℃ in this thesis. For the MIS-capacitors C-V measurement, the parallel mode was selected due to a high series resistance existed. Note that, the AC gate signal with a variation rate of dv_{ac}/d_t was applied and the corresponding current (i_{ac}) flowing across the MIS-capacitor was measured. The capacitance of the MIS-capacitor was determined by Eq. (2.6), which was calculated by Keysight B1500A automatically.

$$C = \frac{i_{ac}}{dv_{ac}/dt} \qquad (2.6)$$

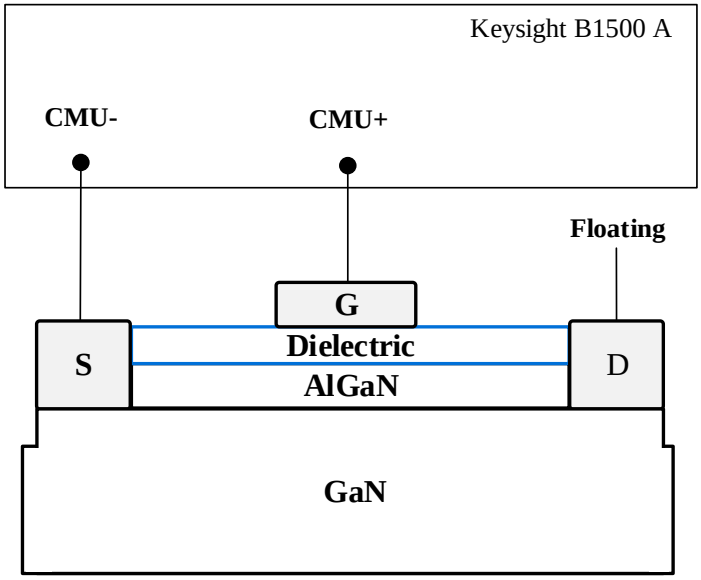

Fig. 2.9 The measurement circuit for the C-V measurement

The TDDB measurement was carried out using one HRSMU and one GNDU on the power device analyzer Keysight B1505A. The MIS-transistors were probed by a probe station, and the measurement circuit is illustrated as Fig. 2.10. The HRSMU was connected to the gate, the GND was connected to the source, and the drain was floating. The gate was stressed at constant high positive voltage biases, where the gate voltage

biases should be larger than 70% of the maximum tolerable gate bias, but be smaller than 90% of the maximum tolerable gate bias. The gate currents were sampled by the HRSMU once per second, and the breakdown time was defined at the critical point when the gate leakage increased to the compliance current of 1 mA.

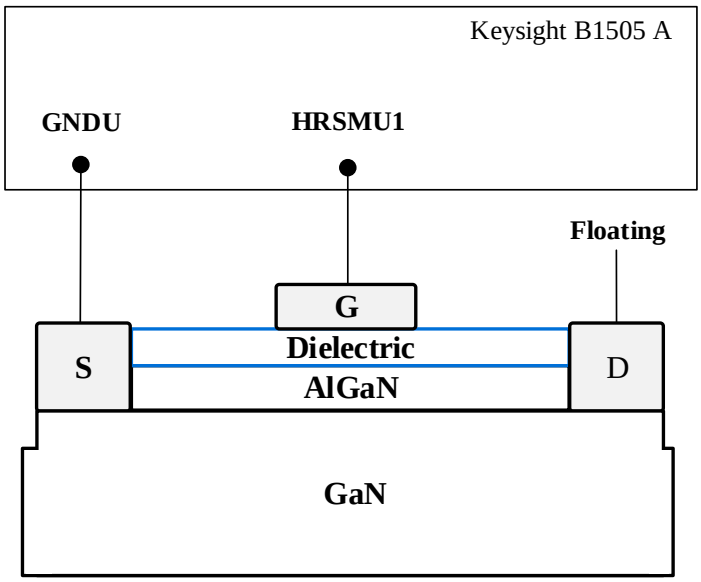

Fig. 2.10 the measurement circuit for the TDDB measurement.

The PBTI measurement was carried out using two HRSMUs and one GNDU on the power device analyzer Keysight B1505A. The measurement circuit is illustrated as Fig. 2.11. The source of MIS-transistor was connected to the GNDU, the gate and the drain were connected to the two HRSMUs. A positive bias was first applied to the gate of devices, both drain and source were grounded. After that, an I_D–V_{GS} measurement was carried out to monitor the V_{th} shift, and the change of transfer characteristics was monitored. The gate bias time interval was set as 0, 1, 2.1, 4.6, 10, 21, 46, 100, 210, 460, 1000, 2100, 4600, 10000, and 21000 s. The identical I_D–V_{GS} measurement was carried out after each gate bias finished.

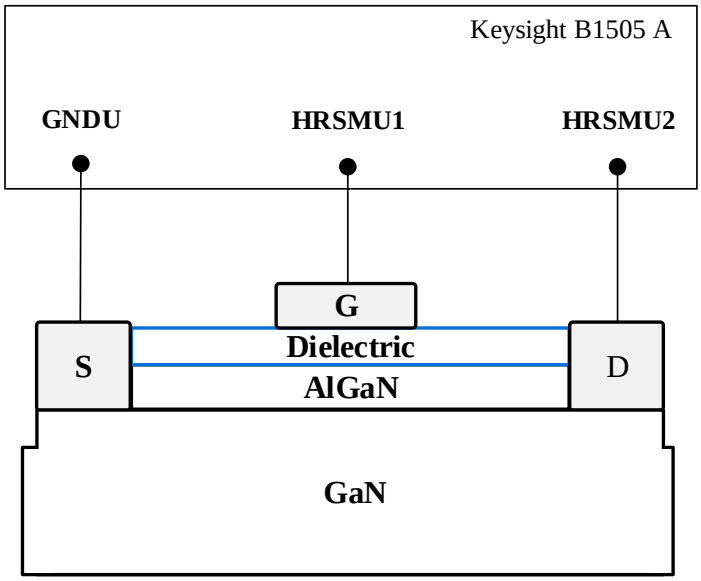

Fig. 2.11 The measurement circuit for the PBTI measurement

The following paragraphs will introduce the background of the current collapse measurement in this study. The GaN-based HEMTs conduct through a 2DEG channel in on-state operation. At the high drain voltage stress conditions, some electrons may get trapped in specific regions of the HEMTs structure, especially at the passivation/barrier layer interface [6]. This leads to an additional electric field, which repels the electrons in the 2DEG channel. Therefore, an increased on-state resistance (R_{ON}) would occur in a fast switching environment and is known as the degradation of dynamic R_{ON} or the current collapse effect. An increased dynamic R_{ON} would lead to a lower dynamic output current and a higher power loss. The GaN-based HEMTs typically are being operated at both hard and soft-switching conditions for power conversion applications. Hard switching condition refers to the overlap of the voltage and current waveforms when HEMTs switch either from on-to-off or off-to-on states [7]. By contrast, the soft switching refers to there is no or minimal overlap of the voltage

and current waveforms. Note that, the hard switching conditions were considered in this study for evaluating the current collapse effect, and the pulsed I-V measurement technique was used to analogize the soft switching operation.

The pulse I-V measurement was carried out using one HRSMU, one high-power source/measure unit (HPSMU), and one GNDU on the power device analyzer Keysight B1505A. The MIS-transistors were probed by a probe station, and the measurement circuit is illustrated as Fig. 2.12. The source of MIS-transistor was connected to the GNDU, the gate was connected to the HRSMU, and the drain was connected to the HPSMU. The schematic timings of voltage signals in current collapse measurements is demonstrated in Fig. 2.13 [8]. The measurement started from the off-state bias. The quiescent gate bias ($V_{GS,\,Q}$) was fixed at a negative voltage, which should be smaller than the V_{th} for pinching off the 2DEG channel. The quiescent drain biases ($V_{DS,\,Q}$) were set at high voltages to form high electric fields at the drain side. The off-state stress time was set as 1 s in this thesis. Theoretically, the off-state to on-state switching speed should be very high in order to reduce the de-trapping effect before the dynamic R_{ON} extraction. This dynamic R_{ON} is compared to the initially measured static R_{ON} to see if any change has occurred due to the high drain voltage stress. Owing to the limited switching speed and maximum output voltage of SMUs, the pulsed output curves were measured at 500 μs after the off-state voltage stresses. The on-state was featured at a fixed positive $V_{GS,}$ which is larger than the V_{th}. Note that, the pulsed output curves at on-state should be sketched by connecting the drain current density at each positive drain bias, but not by implementing an I_D-V_{DS} sweep after off-state voltage stress.

Otherwise, an underestimation on the drain current collapse would occur.

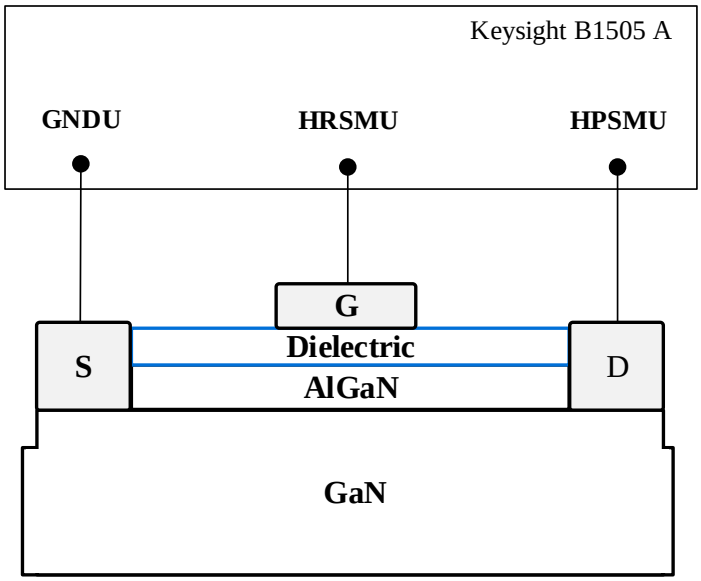

Fig. 2.12 The measurement circuit for the current collapse measurement

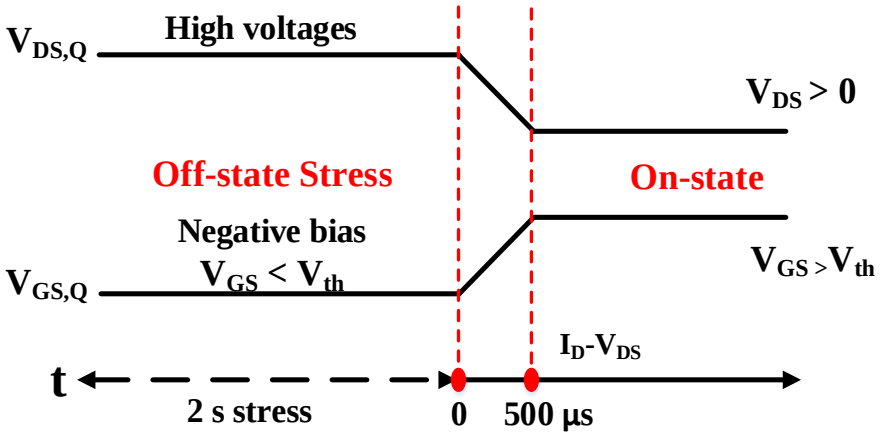

Fig. 2.13 The schematic timings of voltage signals in current collapse measurement

The off-state breakdown voltage measurement was carried out using one high-voltage source/measure unit (HVSMU), one HPSMU, and one GNDU on the power device analyzer Keysight B1505A. The MIS-transistors were probed by a probe station, and the measurement circuit is illustrated as Fig. 2.14. The source of MIS-transistor

was connected to the GNDU, the gate was connected to the HPSMU, and the drain was connected HVSMU. The gate bias was fixed at a negative voltage, which should be smaller than the V_{th} for pinching off the 2DEG channel. The drain signal was swept from 0 V to the maximum tolerable drain bias. The sweeping resolution was set as 1 V, and the sweeping interval time was set as 100 ms. The compliance currents of HPSMU and HVSMU were set a 1 mA for protecting the measurement system.

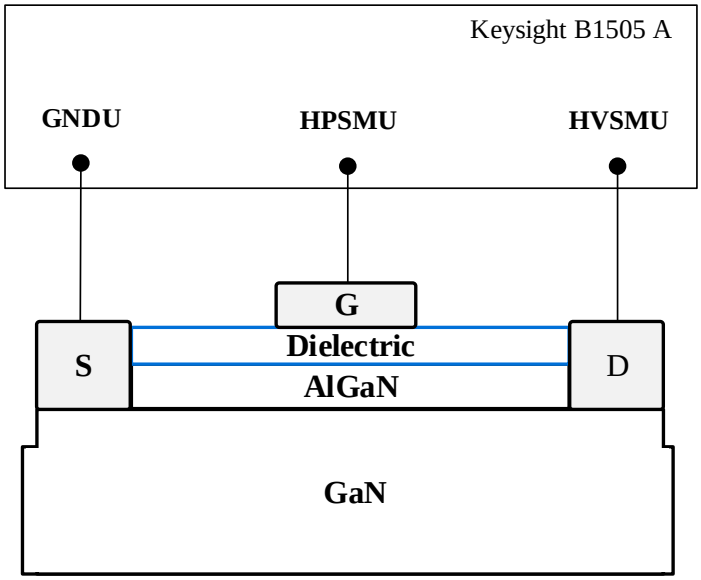

Fig. 2.14 The measurement circuit for the off-state breakdown voltage measurement

The atomic composition on the GaN surface was investigated by XPS, which utilized incident X-ray to induce the photoelectron effect on the GaN surface. The XPS measurements were implemented in an AMICUS system consisting of an Mg/Al *K*α Xray source and an electron energy analyzer. The X-ray is capable of exciting the electrons at the core levels to escape from the GaN surface, then the electrons with selected energy can be collected. The produced electron energy spectra were compared with the energy spectrum database to decide the atomic composition and the bonding

on the GaN surface. Here, the Ga 3d spectrum was fitted by using the Avantage surface analysis software.

2.4 References

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CHAPTER 3 Surface treatments on AlGaN/GaN devices with Al_2O_3 gate dielectric

3.1 Introduction

AlGaN/GaN HEMTs suffer from large gate leakage currents due to Schottky-gate contacts [1]. By replacing the Schottky-gate contact with a metal-insulator-semiconductor (MIS) structure, gate leakage currents can be suppressed significantly. High-*k* dielectrics, such as Al_2O_3[2], HfO_2 [3], CeO_2 [4], and ZrO_2 [5] have been considered for MIS gate structures in the GaN-based devices. The gate dielectric material should exhibit wide band offsets to the GaN in order to form a barrier for both electrons and holes. The Al_2O_3 with a large conduction and valence band offsets (2.05 eV and 1.08 respectively) [6] to the GaN and a high relative permittivity (~9) [7] was chosen in this study. However, a high interface trap density of $\sim 1\times10^{13}$ $cm^{-2}eV^{-1}$ at the Al_2O_3/GaN interface has been reported [8]. This poor interface quality has been associated with the native gallium oxide and dangling bonds on the GaN surface [9], resulting in large leakage currents and the V_{th} instability.

In order to reduce the interface state density, GaN surface treatments have been suggested as critical procedures to remove native oxide on the GaN or to passivate the GaN surface prior to dielectric deposition. The surface cleaning with HCl [10] or HF [11] is commonly used to eliminate the native oxide, but the exposed GaN surface suffers from re-oxidation before dielectrics deposition. Sulfide-based passivation schemes, such as aqueous $(NH_4)_2S$ solution, are capable of protecting the GaN surface

from immediate re-oxidation by forming Ga-S bonds [12]. However, metal contamination of the $(NH_4)_2S$ solution and the limited stability of the $(NH_4)_2S$ passivation during the fabrication process [13] are two limitations, which might be detrimental to devices performance. In contrast, a recent study [14] reported that the surface preparation using sacrificial 1-Octadecanethiol (ODT) self-assembled monolayer (SAM) could protect insulator/GaAs interfaces from interfacial oxides. The surface passivation by using ODT SAMs can improve the sulfide passivation stability in an air ambient environment [15]. In addition, studies have reported that oxidation of the GaN surface is able to fill up the Ga dangling bonds, and form high-quality Ga-oxides on the GaN surface [16]. Among these oxidation methods, the oxygen plasma technique has been found to be a practical approach to passivate the dangling bonds and remove possible carbon contamination on the GaN surface [17]. Therefore, both the removal of the native oxide on the GaN surface and the passivation of the GaN surface by Ga-S and Ga-O bonds are regarded as effective methods to reduce the interface state.

In this Chapter, a low-cost and effective method of the ODT treatment is proposed to improve the Al_2O_3/GaN interface quality. The chemical composition on the GaN surface with different treatments and the electrical characteristics of MIS devices with ALD-Al_2O_3 gate dielectric have been studied. In addition, comparisons have been made among the samples without any treatment and with the HCl, oxygen plasma, and ODT treatments prior to the gate dielectric deposition. It is important to point out that the main objective in this Chapter is to reduce the Al_2O_3/GaN interface states density by

using surface pre-treatment techniques and to fabricate AlGaN/GaN MIS-HEMTs with satisfied sub-threshold characteristics and a high threshold voltage stability.

3.2 AC C-V Simulation of AlGaN/GaN MIS-capacitors

The TCAD simulation was carried out to understand the C–V behavior of oxide/AlGaN/GaN MIS-capacitors, where the gate dielectric/AlGaN interface state had been taken into account. In the simulation, a numerical solver of the Poisson equation based on the one-dimensional Gummel algorithm was used to calculate the C-V curves, the 2DEG density was assumed as $9x10^{12}$ cm^{-2}, and the AC signal was assumed to be a constant frequency of 1 MHz. As shown in Fig. 3.1, a characteristic C–V curve of oxide/AlGaN/GaN structure with two steps is observed, which is peculiar to the MIS structure fabricated on the heterostructure. The maximum capacitance plateau ($C_{OX)}$ at the forward bias corresponds to the insulator capacitance. Another capacitance plateau at the reverse bias (C_{Total}) is determined by the series capacitance of the insulator and barrier layers. At a deep reverse bias, the capacitance steeply decreases to nearly zero, indicating the 2DEG depletion at the AlGaN/GaN interface. The C_{OX} and C_{Total} can be expressed as,

$$C_{OX} = \frac{\varepsilon_r \varepsilon_o}{d} \qquad (3.1)$$

$$C_{Total} = \frac{C_{ox} \times C_B}{C_{ox} + C_B} \qquad (3.2)$$

where ε_r is the relative permittivity of the gate dielectric increases, ε_o is the permittivity of vacuum, d is the thickness of gate dielectric, C_B is the capacitance of the AlGaN barrier layer.

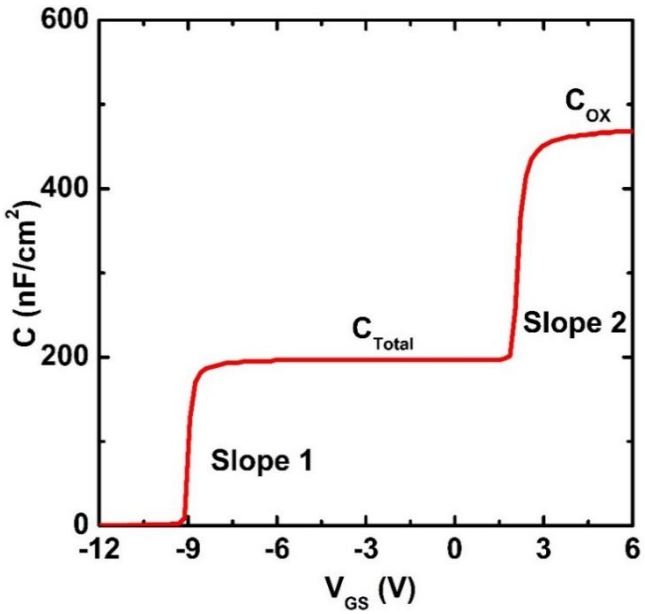


Fig. 3.1 A typical C-V curve of the oxide/AlGaN/GaN MIS-capacitor

In the real case, the interface traps are commonly located at the oxide/GaN cap layer interface originating from structural defects, metal impurities, or N vacancies on the GaN surface. These interface traps have energy states in the GaN bandgap which allows them to exchange charges with the GaN cap layer in a short time. Interface states can be charged or discharged by applying appropriate surface potential. As shown in Fig. 3.2, the interface traps distributions in the simulation were assumed to be three types. The charge neutrality level $E_i \approx E_C$ -1.6 eV is a branch point for acceptor- and donor-like interface states having a U-shaped distribution, which is in accordance with the disorder-induced gap state model. For the case with the high interface traps density, the traps concentration at the band edges and in the middle of the gap were assumed as

$1x10^{14}$ and $3.3x10^{13}$ $cm^{-2}eV^{-1}$, respectively. For the modeling of the structure with relatively low interface traps density. The traps concentration at the band edges and in the middle of the gap were assumed as $3.3\ x10^{13}$ and $1\ x10^{12}$ $cm^{-2}eV^{-1}$, respectively. Moreover, according to the studies in ref [18], the donor-like traps remain empty independent of the bias sweeping due to their deep energy level. For electrons emission from the acceptor-like traps, the Shockley-Read-Hall statistics should be taken into account. E_{Tm} is the deepest energy of the state which can respond the ac signal during the C-V sweeping time, it can be described as :

$$E_{Tm} = kTln(\sigma N_C v_{th} t_{meas}) \qquad (3.3)$$

where k is the Boltzmann constant, T is the temperature, and σ is the capture cross section, N_C is the effective density of states, v_{th} is the thermal velocity of electrons and t_{meas} is the sweeping interval, respectively. E_{Tm} was estimated to be ~0.8 eV from the conduction band at the oxide/GaN interface, indicating only the interface traps in the energy level from E_C to $E_C - 0.8\ eV$ can be affected by the gate voltage sweep. Due to the long emission time constants, the deep acceptor-like traps located from $E_C - 0.8\ eV$ to E_i are unable to de-trap electrons and they act as negative fixed charges leading to a forward V_{th} shift [19].

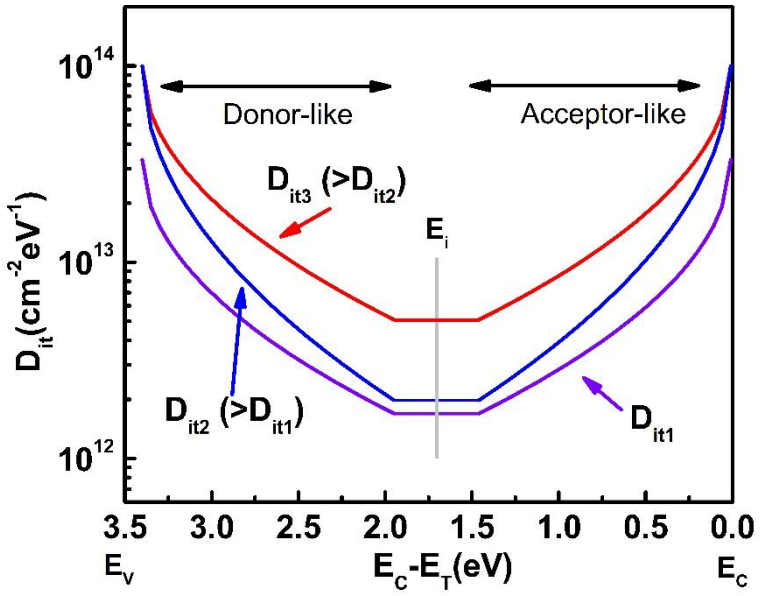


Fig. 3.2 Interface traps distributions used in the simulations: parabolic distribution with a low density of interface trap and parabolic distribution with a high density of interface trap.

The simulated C–V curves are shown in Fig. 3.3 that was similar to the results in a recent publication [18]. Note that, the gate dielectric was chosen as a 20 nm Al_2O_3 in the simulation. The ideal C-V curve (solid line in black) shows a two-step capacitance change, and the three dashed lines show the C-V curves assuming the three parabolic distributions, D_{it1}, D_{it2}, and D_{it3}, respectively. When $V_G > V_{th}$, the 2DEG channel is formed. The first slope in C–V appears, the measured capacitance is the Al_2O_3 dielectric capacitance in series with the AlGaN barrier capacitance. The conduction band keeps moving toward the Fermi level at the Al_2O_3/GaN interface with increasing V_G. As shown in Fig. 3.4(a), when V_G is not high enough, the interface traps at the Fermi level are too deep to respond to the AC signal.

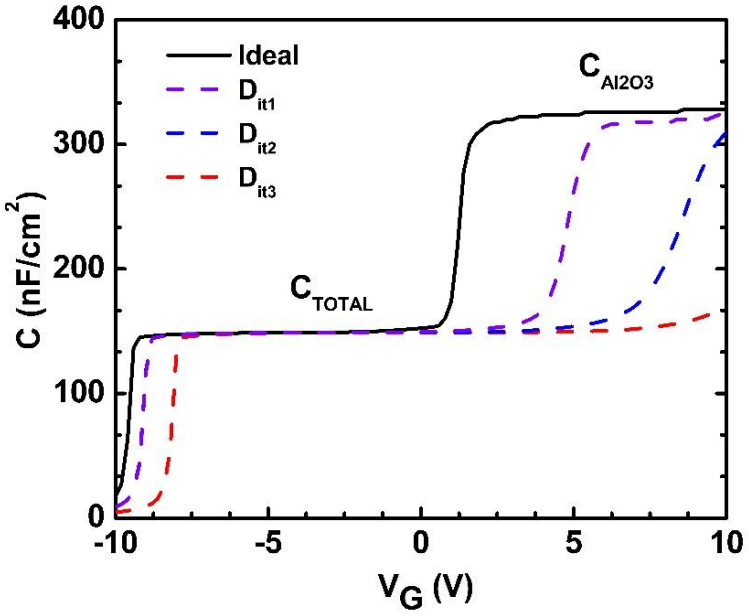


Fig. 3.3 C–V for an ideal structure without interface traps, and with a parabolic distribution of traps.

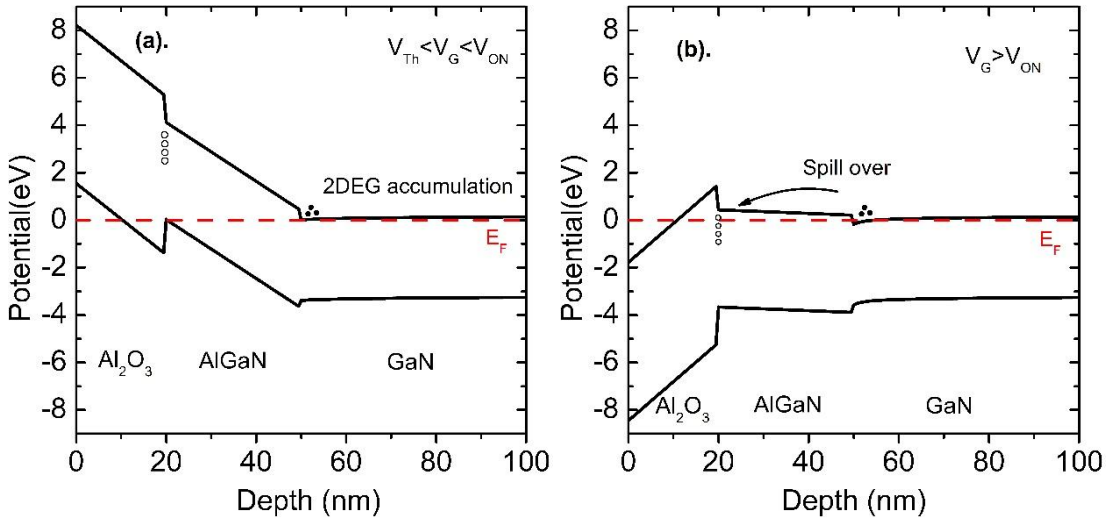


Fig. 3.4 The simulated schematic band diagrams of the metal/Al_2O_3/AlGaN/GaN gate stack with (a) $V_{th}<V_G < V_{ON}$ and (b) $V_G > V_{ON}$.

At the forward bias, the nearly-flat potential of the AlGaN layer is shown in Fig. 3.4 (b) can lead to the electron transfer with ease from the AlGaN/GaN interface to the Al_2O_3/AlGaN interface. Before the electron spill over to the Al_2O_3/AlGaN interface, the traps are unoccupied, and the measured capacitance is C_{Total}. The AlGaN barrier

layer includes a very low electron density of in the simulation. Once the electron spill over to the Al_2O_3/AlGaN interface, the electron would be trapped by the interface state. The electron density in the AlGaN barrier layer increases to over $1x10^{12}$ cm^{-3} at the same time. The leakage current through the barrier layer becomes significant, the Al_2O_3/AlGaN interface and the 2DEG channel are shorted out gradually, resulting in the second C–V slope. In the forward bias region, the C–V slope drastically decreases with increasing interface state density. In the actual case, electron trapping at the Al_2O_3/AlGaN interface states is highly probable. The acceptor-type states result in excess negative charges when they trap electrons. Such negatively charged interface states can screen the gate electric field, suppressing the potential modulation of the AlGaN layer, this causes the stretch out of the C–V curve. In an extreme case, if an MIS device includes very high interface state densities (D_{it3}), then the second step will not be observed even at high forward bias. Indeed, several papers showed no C–V step even at high forward bias [20, 21]. In addition, it can be observed that the C-V slope at the negative bias would be more positive if a higher D_{it} existed at the Al_2O_3/AlGaN interface. As discussed above, the deep acceptor-like interface traps act as negative fixed charges during the C-V sweeping, hence a higher D_{it} leading to a more positive C-V slope shift.

3.3 The detailed fabrication process of the GaN MIS-devices with different surface treatments

The flowchart of the MIS-devices fabrication process is demonstrated in Section 2.2. The cross-sectional view of the fabricated GaN-based MIS-devices is shown in Fig. 3.5 The investigated GaN-based material stack consists of a 1 nm undoped GaN cap layer, a 22 nm thick $Al_{0.25}Ga_{0.75}N$ barrier layer, a 0.33 μm GaN channel layer, and a 5.4 μm highly resistive GaN buffer on a Si substrate.

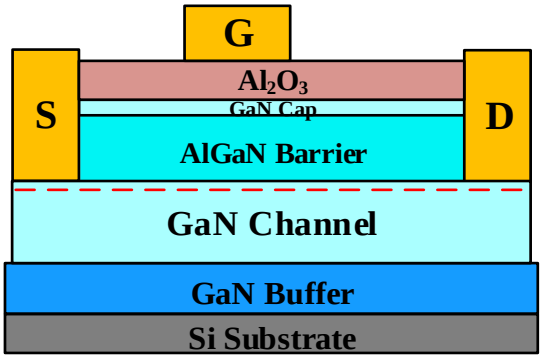


Fig. 3.5 Schematic cross-sectional view and top view of the fabricated MIS-devices

Firstly, the Au-free source and drain were formed by e-beam evaporation of Ti/Al/ Ti/TiN (25/125/45/55 nm) patterned by a photolithography and a lift-off technology, and annealed at 840 ℃ in N_2 ambient for 40 s by RTA. After the formation of ohmic contact, the mesa isolation region was formed by BCl_3/Cl_2 ICP etching. After the organic cleaning processes, sample A was without any treatment. Samples B, C and D were treated in 2 mol/L HCl solution at room temperature for 5 min to remove the native oxide. In addition, sample C was subjected to O_2 plasma in a reactive ion plasma system with a low RF power of 50 W and an O_2 flow of 50 sccm for 3 min. Sample D was

immersed in a 5 mM ODT in ethanol at RT for 24 hours to passivate the GaN surface. Note that the GaN surface was hydrophilic after HCl cleaning but become hydrophobic during the ODT treatment due to the alkyl termination of the ODT molecule. In order to ensure the GaN surface was passivated by the ODT monolayers in saturated, the 24 hours immersion time was used in this study. After the ODT exposure, sample D was immersed in ethanol and ultrasonically cleaned for 10 min followed by N_2 drying. Furthermore, before the ALD, sample D was exposed to 30 H_2O pulses with the same pulse/purge duration as used in the ALD process at 260 ℃ in the ALD reactor, to in situ cleave the S-C bonds of ODT SAM. Fig. 3.6 show the 2-D structure of the ODT molecule, which consists of the sulfhydryl group connected with an n-octadecyl chain.

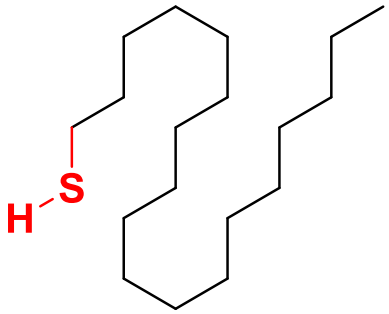


Fig. 3.6 The 2-D structure of ODT molecule

After that, the Al_2O_3 films with a nominal thickness of 20 nm were grown by ALD with TMA as the precursor and H_2O as the oxidant source. The 180 ALD cycles were run at 260 ℃ at a chamber pressure of ~50 Pa. High purity N_2 (20 sccm) was used as the precursor carrier and purge gas. The thickness of Al_2O_3 was determined by spectroscopic ellipsometry and found to be close to a nominal value of 20 nm. After local Al_2O_3 removal with 1% HF, another photolithography process was used to define

Ni/TiN (50/100 nm) gate electrodes. The chemical property on the GaN surface was investigated by XPS, and the electrical properties were measured by using an Agilent B1500A semiconductor analyzer.

3.4 X-ray Photoelectron Spectroscopy (XPS) for the GaN surface characterization

The XPS analysis was conducted to investigate chemical composition variation on the GaN surface induced by different treatments. The XPS measurements were implemented in an AMICUS system consisting of an Mg/Al *K*α Xray source and an electron energy analyzer, and the detection depth was expected to be within 5 nm. Moreover, the interval time before the XPS measurement was approximate 8 hours. Fig. 3.7 shows the deconvoluted *core level* (CL) spectra of Ga 3d for the four samples: A - no treatment, B - HCl, C - O_2 plasma, and D - ODT. The carbon (C) 1s peak of adventitious carbon (284.8 eV) was used for calibration. XPS data were analyzed after Shirley background subtraction and the Savitzky-Golay smoothing process. The peaks were fitted by using the Gaussian-Lorentz Mix function. According to the XPS analysis in a recent study [12], the Ga 3d spectrum can be decomposed as a main component at 19.7 eV related to the Ga-N bonds in the substrate and an additional peak at higher binding energy (20.4 eV) associated with the Ga-O bonds.

The Ga 3d spectrum of the non-treated sample in The XPS measurements was implemented in an AMICUS system consisting of an Mg/Al *K*α Xray source and an

electron energy analyzer, and the detection depth was expected to be within 5 nm. Moreover, the interval time from surface treatments to the XPS measurement was no longer than 8 hours. Fig. 3.7 (a) exhibits a high Ga-O sub-peak, and this indicates the existence of amorphous native oxide at the Al_2O_3/GaN interface. The HCl solution is reported to effectively remove the native oxide on the GaN surface [22]; however, the Ga-N and Ga-O bonds intensity were very similar in Fig. 3.7 (a) and Fig. 3.7 (b). The possible reason is that the HCl-treated GaN surface sample has been exposed to air and the re-oxidation occurred before the ALD process. The Ga 3d centroid peak of the O_2 plasma treated sample is shown in Fig. 3.7 (c) was shifted to higher binding energy for approximately 0.2 eV when compared to the non-treated sample. In this case, a broader centroid peak is visible with a larger fitted Ga-O sub-peak, which is mainly due to the GaN-cap layer being oxidized and GaO_x formed on the surface [16]. Moreover, ~0.6 nm GaN-cap layer is predicted to be oxidized after the O_2 plasma treatment, which is verified by measuring the etching depth on the AlGaN/GaN heterostructure with a multi-cycle digital etching process (O_2 plasma followed by a 2M HCl immersion). Hence, it can be deduced that the O_2 plasma treatment effectively filled the N vacancies with oxygen atoms, where carrier trapping could be induced. In addition, it is noticed that the O_2 plasma treatment has removed the carbon contamination on the GaN, which corresponds with a lower carbon/nitrogen ratio of 1.1 when compared with a value of 1.6 for the ODT treated sample. Moreover, The sulphur/nitrogen ratio for the non-treated sample, the O_2 plasma treated sample and the ODT treated sample was 0.7, 0.7 and 1.3, respectively.

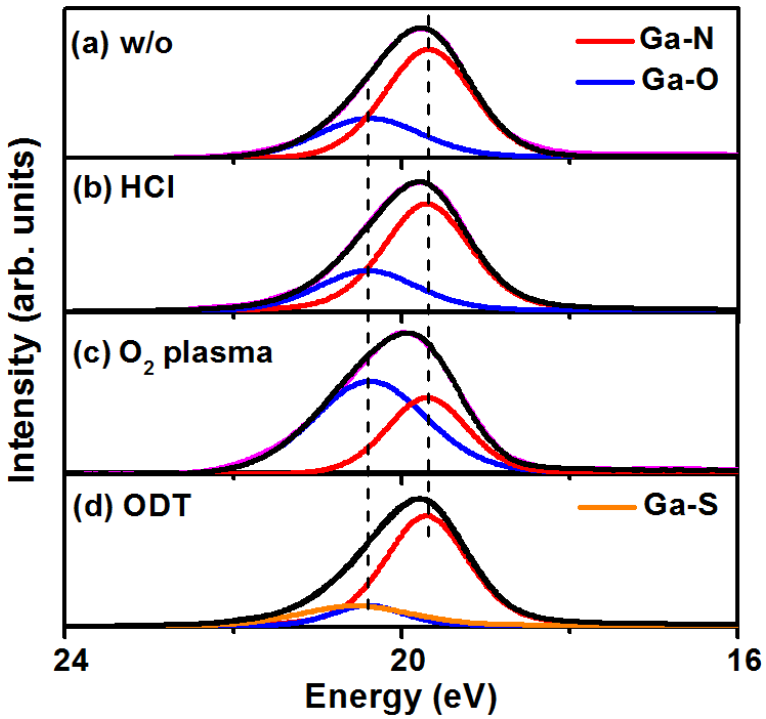


Fig. 3.7 The XPS spectra of Ga 3d CL for samples: (a) A – without treatment; (b) B – with the HCl; (c) C – with the O_2 plasma; (d) D – with the ODT for 24 h

The Ga 3d spectrum of the ODT treated sample in Fig. 3.7 (d) shows a slightly higher binding energy (BE) of the centroid peak than that of the non-treated sample. The fitted Ga-O sub-peak component appears to be reduced, indicating the amount of oxide on the GaN surface has been decreased. There is an extra deconvoluted sub-peak in the Ga 3d CL spectrum at the BE of 20.6 eV, which corresponds to the bond formation between gallium and sulphur atoms [12]. It suggests that the ODT treatment can suppress the oxidation of the GaN surface by forming Ga-S bonds before the subsequent Al_2O_3 deposition. Furthermore, the Ga-S bonds remained at the surface after exposure to thermal H_2O vapor pulses during the ALD process, which indicates that the Ga-S bonds are thermally stable at least up to 260 ℃, in agreement with previous studies

[23], stating that the Ga-S bonds remain stable up to 400 ℃. Hence, it can be deduced from the XPS study that the ODT self-assembled monolayer is capable of providing good passivation of the GaN surface even during high temperature fabrication process, and this feature could allow integration of the ODT treatment into the MOSFET process flow.

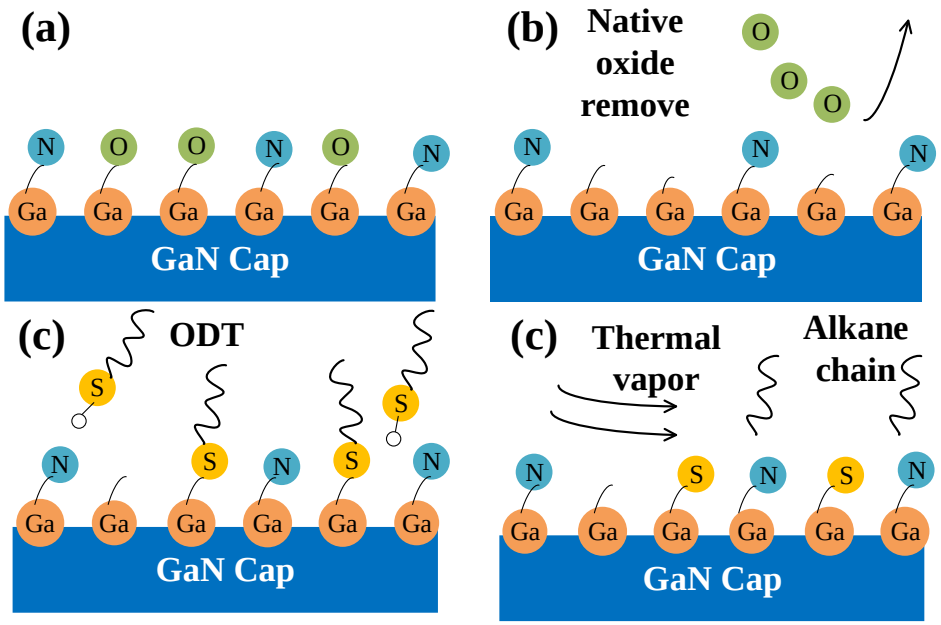


Fig. 3.8 Schematic of the ODT treatment procedure. (a) The non-treated GaN cap. (b) The HCl treatment remove the native oxide. (c) The formation of a dense ODT SAM on the HCl-cleaned GaN. (d) The in vacuo thermal vapor removal of the carbon chain, leaving S atom behind.

Fig. 3.8 shows the schematic of the chemical composition on the GaN surface during the ODT treatment. Firstly, the wet chemical etching in 2M HCl is used to remove the native oxide on the GaN wafer (Fig. 3.8 (b)). Secondly, by immersing the wafer in the ODT solution at RT for 24 hours, the GaN surface is left with the ODT SAM (Fig. 3.8 (c)). The presence of chemisorbed Ga-S bonds on the GaN surface depicted in the schematic in Fig. 3.8 (c) can be proven by the XPS results and a clear

signature of Ga-S sub-peak shown in Fig. 3.8 (d). Thirdly, the exposure of the surface to H_2O vapor at 260 ℃ in the ALD reactor led to the removal of the alkane chain of the ODT SAM. This alkane chain reduction may be attributed to the thermal cleavage of S-C bonds [14]. Finally, the Ga-S bonds on the GaN surface act as a barrier for suppressing the Ga-O bond formation during the subsequent Al_2O_3 deposition (Fig. 3.8 (d)), which could result in a high-quality interface between ALD-Al_2O_3 and GaN-cap.

3.5 Multi-frequency C-V characterization on the GaN MIS-capacitors

The two rising edges C-V characteristics of the GaN MIS-capacitor is already introduced in Section 3.2. The first rising edge at negative measurement gate voltage (V_G) corresponds to the formation of the 2DEG channel, and the second rising edge at positive V_G refers to the spill-over of the 2DEG at the Al_2O_3/GaN interface [18]. Multi-frequency C-V characteristics of MIS-capacitors with different surface pre-treatments at room temperature (~25 ℃) are shown in Fig. 3.9. The V_G was swept from -14 V to 5 V with a step of 20 mV, and the frequency was varied from 2 MHz down to 1 kHz. The frequency dispersion at the second rising edge has been observed in all samples and a more significant frequency dispersion indicates a higher Al_2O_3/GaN interface traps density [19]. Furthermore, when applying a higher positive gate bias, electrons start to distribute in the barrier AlGaN layer, leading to an increase of capacitance to the Al_2O_3 capacitance. Note that the capacitance plateau at the zero bias of the O_2 plasma treated

sample C is slightly lower than that of the other three samples. This is likely to be due to a thin oxidized GaO_x interlayer forming between Al_2O_3 and GaN-cap after the O_2 plasma treatment, leading to an increase of the equivalent thickness of the gate dielectric. The obvious horizontal frequency dispersion is detected in the second rising edge for samples A, B and C. In contrast, by using the ODT GaN surface treatment (sample D), a rising edge with a smaller frequency dispersion is observed.

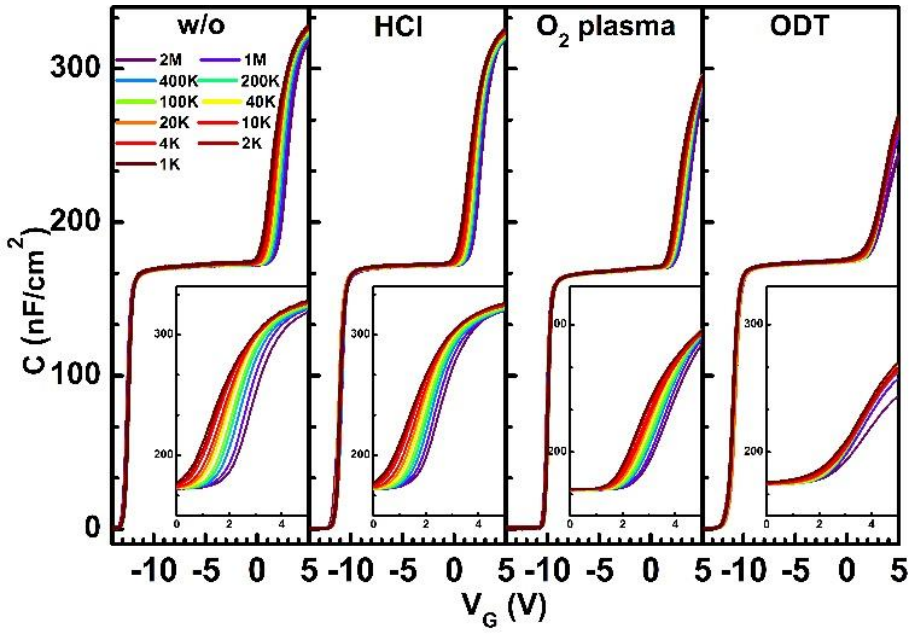


Fig. 3.9 Multi-frequency C-V characteristics of Al_2O_3/GaN/AlGaN/GaN MIS-capacitor structures without (sample A) and with the HCl (sample B), O_2 plasma (sample C) and ODT (sample D) surface treatments.

The Al_2O_3/GaN interface trap density can be calculated by the second slope onset voltage (V_{ON}) in the C-V curves [24]. Note that, when V_G is smaller than V_{ON}, the interface traps at the Fermi level can not respond to the ac signal. When V_G increases to V_{ON}, the electrons start to spill-over from 2DEG to the Al_2O_3/GaN interface, and the

interface traps at the Fermi level can respond to the ac signal by capturing or emitting electrons. This is because the intrinsic frequency of interface traps at the Fermi level is larger than the ac measurement frequency. The onset voltage dispersion (ΔV_{ON}) occurs at two measurement frequencies (f_1, f_2) due to interface traps existing in the energy range from $E_{Trap}(f_1)$ to $E_{Trap}(f_2)$. The detectable energy of the interface trap $E_{Trap}(f_m)$ as a function of measurement frequency f_m can be represented by:

$$E_{Trap}(f_m) = E_C - E_T = kTln\left(\frac{v_{th}\sigma_n N_c}{2\pi f_m}\right) \qquad (3.4)$$

where k is the Boltzmann's constant, T is the measurement temperature, N_C = 2.7×10^{18} cm^{-3} is the effective density of states in the conduction band of GaN, $\sigma_n = 1\times10^{-14}$ cm^2 is the electron capture cross section, and v_{th} = 2×10^7 $cm\cdot s^{-1}$ is the thermal velocity of electrons. An equivalent average energy level of the interface state (E_{AVG}) in the energy range from $E_{Trap}(f_1)$ to $E_{Trap}(f_2)$ can be found as:

$$E_{AVG} = \frac{E_{Trap}(f_1) + E_{Trap}(f_2)}{2} \qquad (3.5)$$

According to the interface state density - energy level mapping method proposed by Yang *et al* [25], distribution of the Al_2O_3/GaN interface states can be obtained by Eq. (3.6):

$$D_{it}(E = E_{AVG}) = \frac{C_{OX}\cdot\Delta V_{ON}}{q\Delta E_{Trap}} - \frac{C_{OX}+C_B}{q^2} \qquad (3.6)$$

where C_{OX} is the capacitance of ALD-Al_2O_3 dielectric, C_B is the capacitance of the AlGaN barrier layer, ΔE_{Trap} is the interface trap frequency dependent energy difference, ΔV_{ON} is the onset voltage frequency dependent shift. The V_{ON} was extracted by reading the voltage when the capacitance reaches 110% of the first plateau capacitance, and the detail is explained in the end of this section. The value of C_{OX} can be extracted as the

maximum capacitance observed in C-V plots in Fig. 3.9, and is found to be 326 nF/cm^2 for the non-treated samples. It is worth noting that the MIS-capacitors have been measured with sweeping the gate bias to a higher voltage of 10 V. The C-V curves of four samples at 1 MHz are plotted in Fig. 3.10. The fresh C-V curves are presented as the lines in black. If using a higher maximum voltage of 10 V to re-measure the same devices, the C-V curves will be shown as the lines in red for each sample.

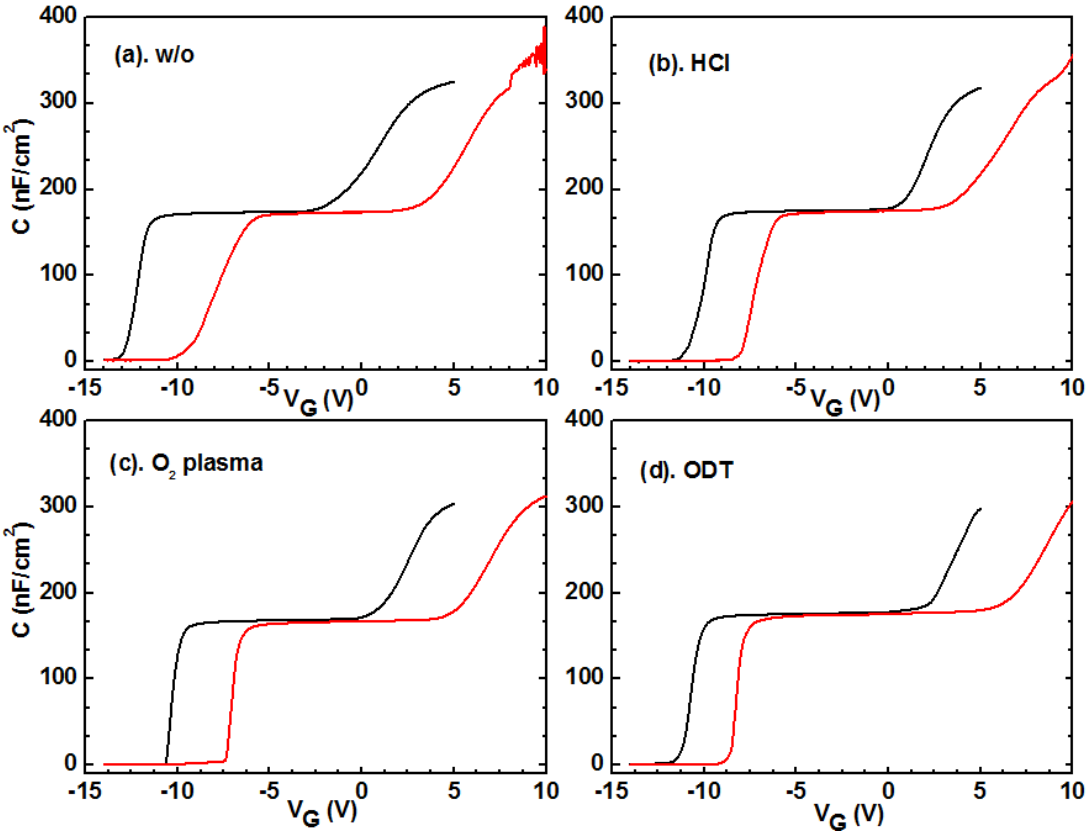


Fig. 3.10 The C-V characteristics of ALD-Al_2O_3/GaN/AlGaN/GaN MIS-capacitors at 1 kHz (a). without and (b). with the HCl, (c). with O_2 plasma and (d). with ODT surface treatments.

A similar phenomenon can also be found in the study [20]. This might be due to a more charge-trapping, at the Al_2O_3/GaN interface and the pre-existing Al_2O_3 bulk traps under excessive forward biases. In addition, a stretch out phenomenon appeared at the

second slope of C-V curves, which could be explained as an increase of the Al_2O_3/GaN interface state density [18, 26], also caused by the large sweep voltage of 10 V. As a result, a large bias voltage could act as electric stress on the gate that would generate more defects at the Al_2O_3/GaN interface [27] and the Al_2O_3 bulk. Therefore, we used -10 V to 5 V as the sweep voltage for the CV measurement to estimate the as-grown interface defects. In addition, the permittivity of the Al_2O_3 film in this study is estimated as ~7.5, which is lower than the expected theoretical value (~9). This is because that the Al_2O_3 deposited by thermal ALD is reported with a lower mass density due to the incorporation of OH groups into the Al_2O_3 film [28]. The maximum capacitances were extracted from the C-V curves at 1 kHz to avoid the low frequency limit effect [29]. C_B was calculated from the first plateau capacitance in Fig. 3.9, as the latter refers to the series capacitance connection between C_{OX} and C_B. The energy difference of interface states ΔE_{Trap} is described by Eq. (3.7) [25] and can be calculated as:

$$\Delta E_{Trap} = E_{Trap}(f_1) - E_{Trap}(f_2) \qquad (3.7)$$

The frequency dependent onset voltage shift ΔV_{ON} can be extracted using the Eq. (3.8):

$$\Delta V_{ON} = V_{ON}(f_1) - V_{ON}(f_2) \qquad (3.8)$$

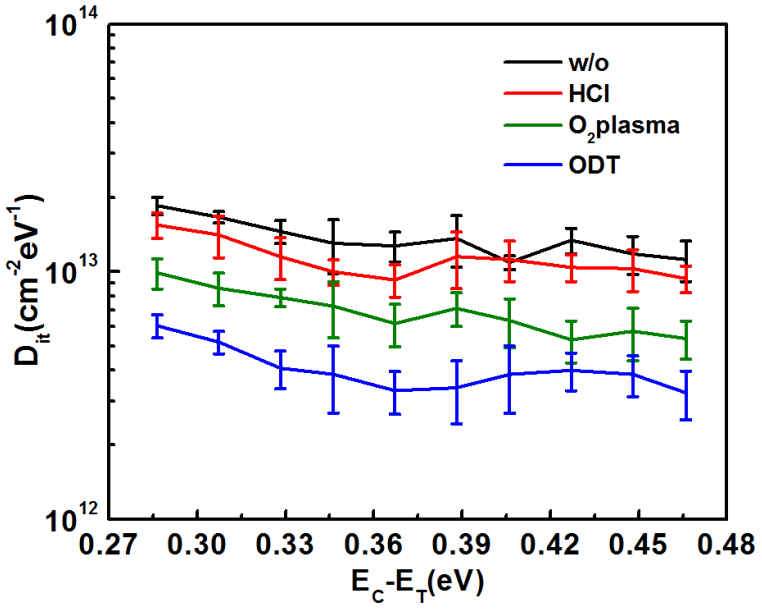


Fig. 3.11 The means value and the standard deviation of the D_{it} distribution of each sample

Fig. 3.11 shows the means value and the standard deviation of the D_{it} distribution of each sample. The electron capture cross section at the interface σ_n was assumed to be 1×10^{-14} cm^2, because the Ref. [30] had reported the capture cross section of the interface traps is in the range from 1.4×10^{-15} cm^2 to 1.4×10^{-14} cm^2 when the traps energy level located from E_C - 0.24 eV to E_C - 0.73 eV. In order to avoid underestimating the interface trap density, we assumed the capture cross section as 1×10^{-14} cm^2, which gives values of D_{it} in the energy level range of 0.3 eV to 0.47 eV from the conduction band edge. For the HCl treated sample, the extracted D_{it} is calculated to be over 9×10^{12} $cm^{-2}eV^{-1}$ in this energy range, which is close to the value of 1.3×10^{13} $cm^{-2}eV^{-1}$ reported in Ref. [31]. This is likely to be due to re-oxidation of the exposed GaN surface before transferring the sample into the ALD chamber. For the O_2 plasma treated sample, D_{it} varies from 9.1×10^{12} $cm^{-2}eV^{-1}$ to 4.8×10^{12} $cm^{-2}eV^{-1}$, when the energy level depth changes from 0.28 eV to 0.47 eV. In comparison, the ODT treated sample shows the

lowest D_{it} distribution among the four samples from 6.1×10^{12} $cm^{-2}eV^{-1}$ down to 3×10^{12} $cm^{-2}eV^{-1}$. The reduction of the interface state density can be explained by the ODT treatment is capable of filling the N vacancies by creating Ga-S bonds, and hence passivate the GaN surface before the ALD process started. Meanwhile, the surface damage of ODT treatment is minimized due to the wet process. Table 3.1 benchmarks the D_{it} results in this work with the state-of-the-art reported values, where the D_{it} refers to the energy level of $E_C - E_T$ = ~0.47 eV. Note that the Al_2O_3/GaN interface state density obtained by using the ODT treatment is close to that reported in the Ref. [9], which is a fairly low interface state density compared with the others up to date reported data. Furthermore, the cost and complexity of using the ODT treatment is much lower than that of the in-site $NH_3/Ar/N_2$ plasma treatment with plasma enhanced ALD-Al_2O_3 gate dielectric.

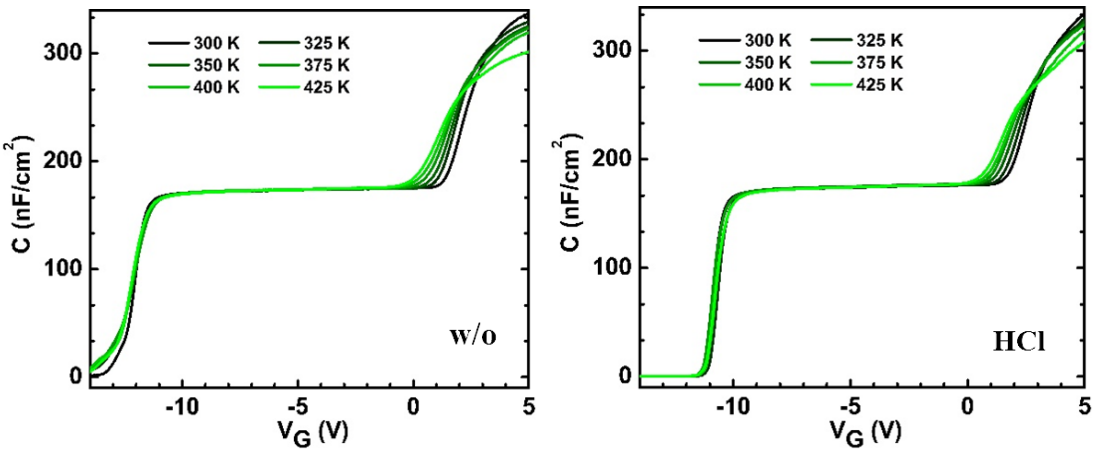
Table 3.1 A summary of the Al_2O_3/GaN D_{it} at E_C–E_T = ~0.47 eV from this work and literature.

Reference	**[9]**	**[25]**	**[32]**	**[33]**	**[18]**	**[34]**	**[35]**	**[36]**	**This work**	**This work**
Dielectric	Al_2O_3	Al_2O_3	Al_2O_3	Al_2O_3	Al_2O_3	Al_2O_3	Al_2O_3	Al_2O_3	Al_2O_3	Al_2O_3
Deposition technique	PEALD	PEALD	ALD	MOCVD	ALD	ALD	ALD	ALD	ALD	ALD
Treatment	In site $NH_3/Ar/N_2$ plasma	In site $NH_3/Ar/N_2$ plasma	UV/ Ozone	HCl	N_2O plasma	In-situ Ar plasma	FG plasma	N_2/O_2 plasma	ODT	O_2 plasma
D_{it} $\times10^{12}$ $cm^{-2}eV^{-1}$	~1	~2.2	~4.1	~7	~9	~30	~30	~38	3.0	4.8

In order to detect the D_{it} with a broader energy range, a multi-temperature CV measurement system had been built, which had been introduced in ref [25]. Similar to the multi-frequency CV measurements, the detectable energy range of the interface states ΔE_T as a function of measurement temperature (T_m) is represented by,

$$E_{Trap}(T_m) = E_C - E_T = T_m K ln\left(\frac{v_{th}\sigma_n N_c}{2\pi f}\right) \qquad (3.9)$$

A higher measurement temperature can detect deeper interface states, thus can bring V_{ON} to a smaller value. The onset voltage dispersion (ΔV_{ON}) occurs at two measurement temperatures (T_1, T_2) due to interface traps existing in the energy range from $E_{Trap}(T_1)$ to $E_{Trap}(T_2)$. In the multi-temperature CV measurements, the measurement gate voltage was swept from -14 V to 5 V with a step of 20 mV. The frequency was fixed as a low value of 1 kHz and the temperature was varied from 300 K up to 425 K. The Multi-temperature C-V characteristics of ALD-Al_2O_3/GaN/AlGaN/GaN MIS-capacitors with different surface treatments are plotted in the Fig. 3.12.



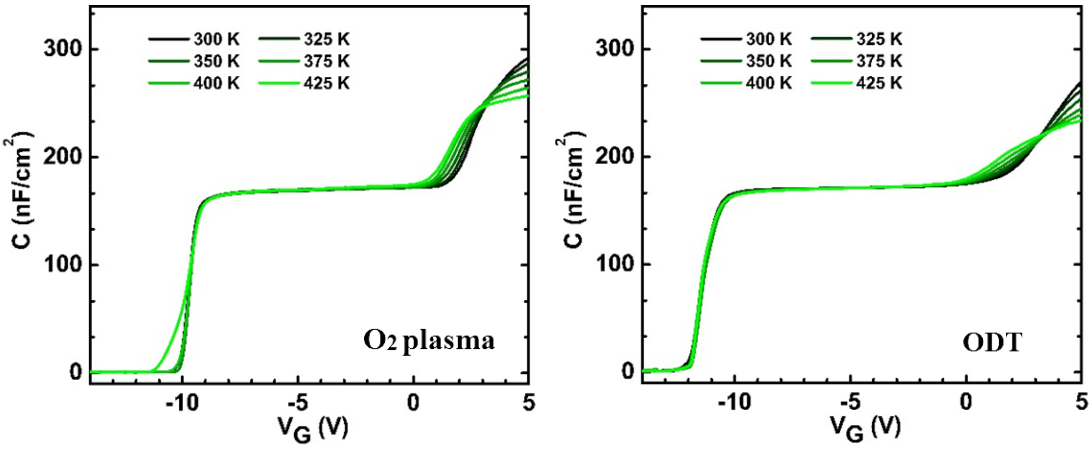


Fig. 3.12 Multi-temperature C-V characteristics of ALD-Al_2O_3/GaN/AlGaN/GaN MIS-capacitor structures without (sample A) and with the HCl (sample B), O_2 plasma (sample C) and ODT (sample D) surface passivation treatments.

When T_m is high (>375 K in our case), the distributive effect at the second C-V slope becomes non-negligible and can substantially distort the C-V behaviors. Similar features have also been observed in another report [37]. This can be explained as the carrier mobility of 2DEG degraded at high temperatures, thus the channel resistance from the source electrode to the gate region was increased. At a higher temperature, the potential distribution under the gate region is more non-uniform, the frequency-dispersions at the second slope are not only caused by the ac response of interface traps at various energy levels. To avoid the estimation error of the D_{it}, the maximum *T*m was set as 425 K in this study.

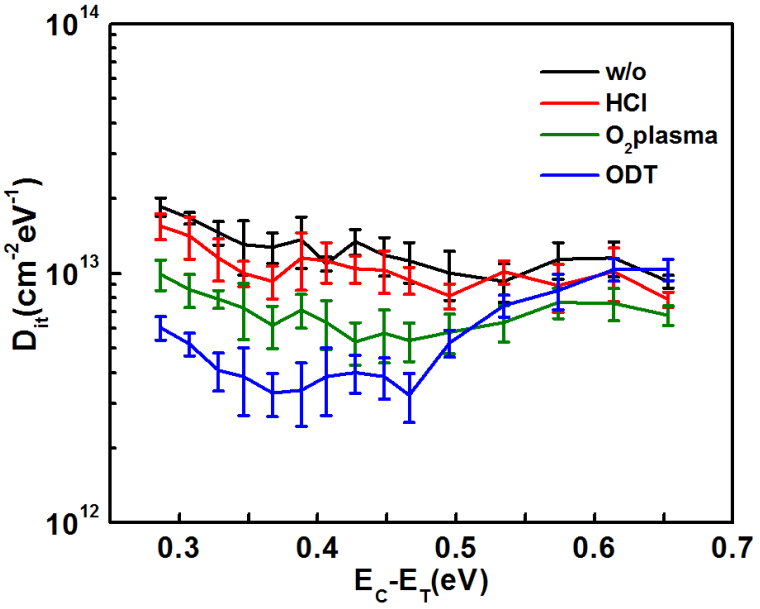


Fig. 3.13 The means value and the standard deviation of the D_{it} distribution of each sample (E_C - E_T = 0.27 eV~ 0.67 eV).

The D_{it} error bars of each sample in the full-detected energy range from 0.27 eV to 0.67 eV have been plotted in Fig. 3.13, by combining the multi-temperature and multi-frequency CV measurements. We set 425 K as the maximum measurement temperature, because some devices were broken down at a higher temperature, especially for the non-treated devices. According to the error bars on the D_{it} results, the ODT treated sample shows the lowest D_{it} distribution among the four samples in the energy range from 0.27 eV to 0.5 eV. This indicates the shallow D_{it} can be suppressed by the ODT treatment. However, in the deeper energy range (0.5 eV to 0.67 eV), the ODT treated sample shows a higher D_{it} than that of the O_2 plasma treated sample, and it is comparable to the results of the HCl treated sample. The ODT-treated sample with more D_{it} at deeper energy level is probably due to carbon impurity on the GaN surface. The carbon related oxide/GaN D_{it} energy level has been predicted to be located near E_C

– 0.54 eV according to a recent study [38]. According to the XPS results, the O_2 plasma treatment has a lower carbon/nitride ratio of ~1.1, when compared with a value of ~1.6 for the ODT treated sample. For the ODT treated sample, a small number of alkane chain may still be left on the GaN surface after the thermal vapor annealing. By contrast, the O_2 plasma treatment is capable of removing carbon impurity content on the GaN surface. This could prove more carbon content existed on the ODT-treated GaN surface, hence a higher density of deep interface traps extracted from the MIS-devices with ODT treatment.

Note that, it is very important to clarify the possible D_{it} estimation error with the C-V method, which would be caused in the measurement. For instance, the gate voltage sweep resolution (V_{RES}) should be low enough, such that $\Delta V_{ON} > V_{RES}$. The study [24] has reported the simulation of the error in D_{it} extraction for different values of V_{RES}. It indicates that the minimum detectable trap density reduces with a reduction in V_{RES}. This study also calculated that the lowest detectable trap density was $\sim 3 \times 10^{12}$ $cm^{-2}eV^{-1}$ for a 30 mV of V_{RES}, with an estimation error of 5%. The V_{RES} of the gate sweep voltage we used in the CV measurement is 20 mV. Another important estimation error could be caused during the calculation of interface state density. The distribution of the Al_2O_3/GaN interface states can be obtained from Eq. (3.6). The parameters C_{OX}, C_B and ΔE_{Trap} in Eq. (3.6) are relatively fixed, and they might have a negligible effect on the estimation error. However, the estimation error possibly occurs at the extraction of the onset voltage shift ΔV_{ON}. Accurate extraction of $V_{ON}(f_m)$ requires a noise-free measurement of a capacitance increase, $C_{ON}(f_m)$, which is to be chosen to be lower than

the capacitance corresponding to the traps. The chosen of $C_{ON}(f_m)$ and the extraction of $V_{ON}(f_m)$ may have an important effect on the D_{it} distribution and values. The $V_{ON}(f_m)$ in the studies [18, 39] is extracted at the cross points of the reverse extension of the second CV slope and the extension of the first CV plateau (C_{Total}). By contrast, the $V_{ON}(f_m)$ in the studies [25, 40] is extracted by reading the voltage when the capacitance reaches approximately 130% of the C_{Toltal}. Moreover, the V_{ON} in our study is extracted by reading the voltage when the capacitance reaches 110% of the C_{Total}. The ΔV_{ON} extraction methods above are demonstrated in Fig. 3.14.

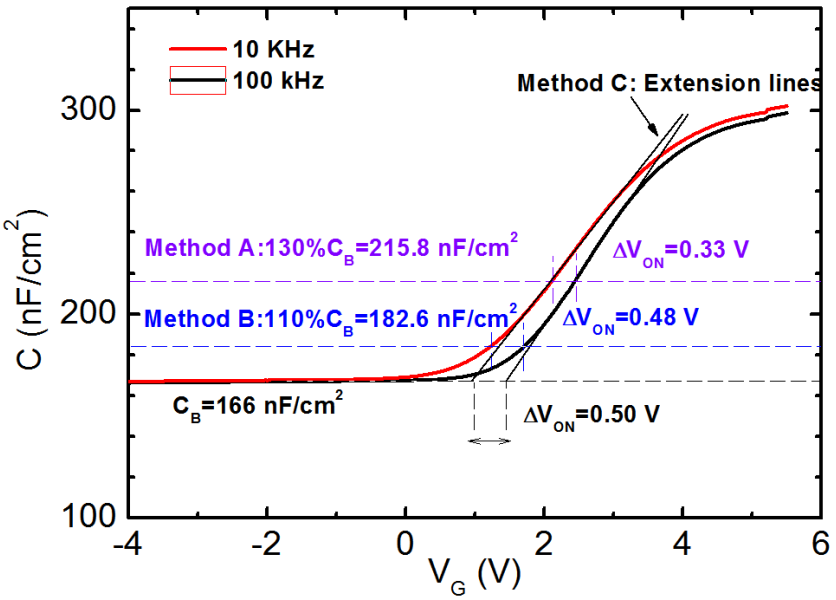


Fig. 3.14 Three types of $V_{ON}(f_m)$ extraction methods

The explanation in the study [25] is referenced to describe the physical mechanisms of traps modulation at onset voltage. Here, the response of interface traps to the ac measurement signal with frequency f_m needs to be analyzed. To facilitate the analysis, the characteristic interface trap frequency is used, which is represented by

$$f_{it} = \frac{1}{2\pi\tau_e} = \frac{\upsilon_{th}\sigma_n N_C}{2\pi}\exp\left(-\frac{E_C - E_T}{KT}\right) \qquad (3.10)$$

where τ_e, υ_{th}, σ_n, and N_C are the electron emission time constants interface traps at energy level E_T, electron thermal velocity, electron capture cross section, and effective density of states in the conduction band in GaN, respectively. When $V_{ON} > V_G > V_{th}$, the 2DEG channel is formed. The conduction band of the barrier layer keeps moving to deeper energy with increasing V_G. When V_G is not high enough ($V_{ON} > V_G$), the interface traps at the Fermi level are too deep to respond to the ac signal. The simulation results are shown in Fig. 3.15(a).

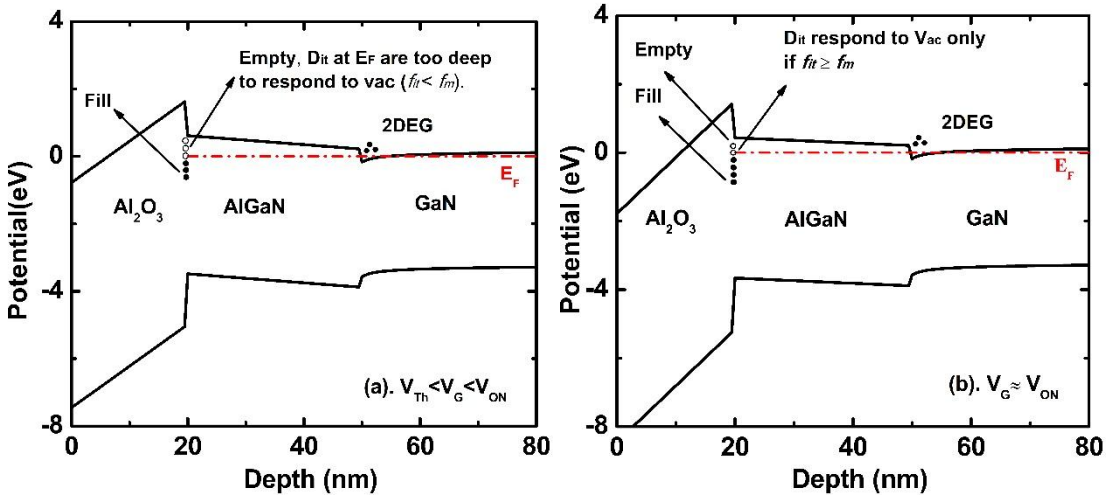


Fig. 3.15 The simulated schematic band diagrams of the metal/Al_2O_3/AlGaN/GaN gate stack with (a) $V_{th}<V_G < V_{ON}$ and (b) $V_G \sim V_{ON}$.

If gate voltage V_G increases to nearly the onset voltage (simulation results are shown in Fig. 3.15(b)), interface traps at Fermi level can respond to ac signal by capturing/emitting electrons only when $f_{it} \geq f_m$ is satisfied. In other words, only the shallower traps near the Fermi level with a larger response frequency can respond to the ac measurement signal. This contributes to additional capacitance and leads to the

second slope in the C–V characteristics. Moreover, frequency dispersion at the second rising slope is observed in our study, when the CV curves measured at different frequency f_m. It is because higher f_m can only detect shallower interface states with a higher f_{it}, thus higher V_G is required to pull down the conduction band toward the Fermi level at the interface. We also simulated the energy band diagrams when V_G was equal to onset voltages at 1 kHz, 10 kHz, 100 kHz and 1 MHz. As shown in Fig. 3.16, the shallower traps near the Fermi level respond to the ac measurement signal at higher f_m, and that requires higher V_G. In other words, higher f_m results in more positive onset voltage. The traps modulation schematic diagrams at 1 kHz and 1 MHz are extracted as shown in Fig. 3.17.

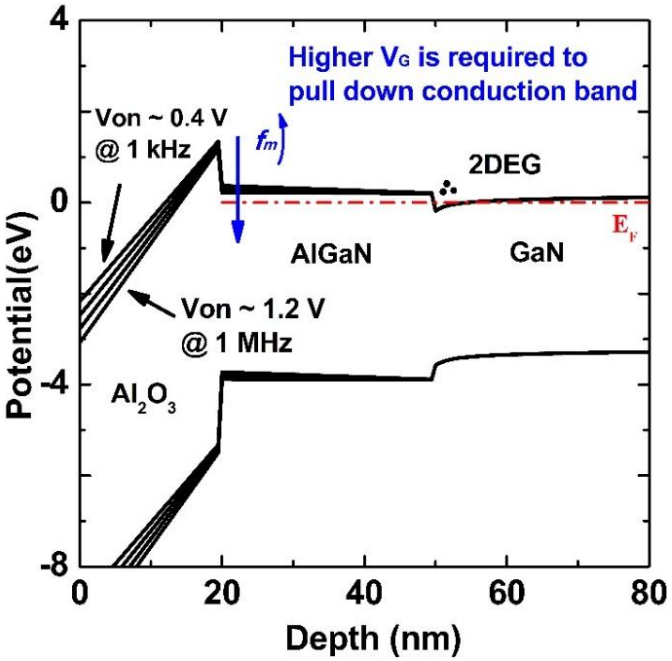


Fig. 3.16 The simulated energy band diagram when V_G equal to onset voltages at different measurement frequencies.

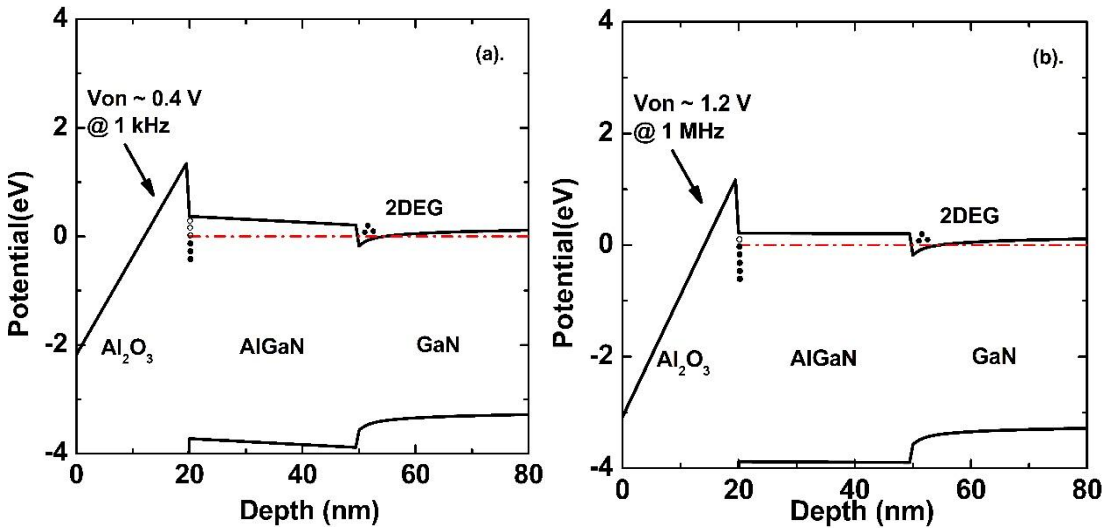


Fig. 3.17 The simulated energy band and traps modulation schematic diagram when V_G equal to onset voltages at (a). 1 kHz and (b). 1 MHz.

Therefore, accurate extraction of onset voltage V_{ON} requires measurement of a capacitance increase, which should be chosen to be close to the first plateau capacitance. However, the evaluation of the capacitance increase at the second C-V step is indeterminate, which may lead to an estimation error. The V_{ON} in our study is extracted by reading the voltage when the capacitance reaches 110% of the first plateau capacitance. The schematic diagram of onset voltage extraction is plotted in Fig. 3.18. The simulated results indicate that the V_{ON} extraction method we used would cause a low underestimation of D_{it}, as shown in Fig. 3.19.

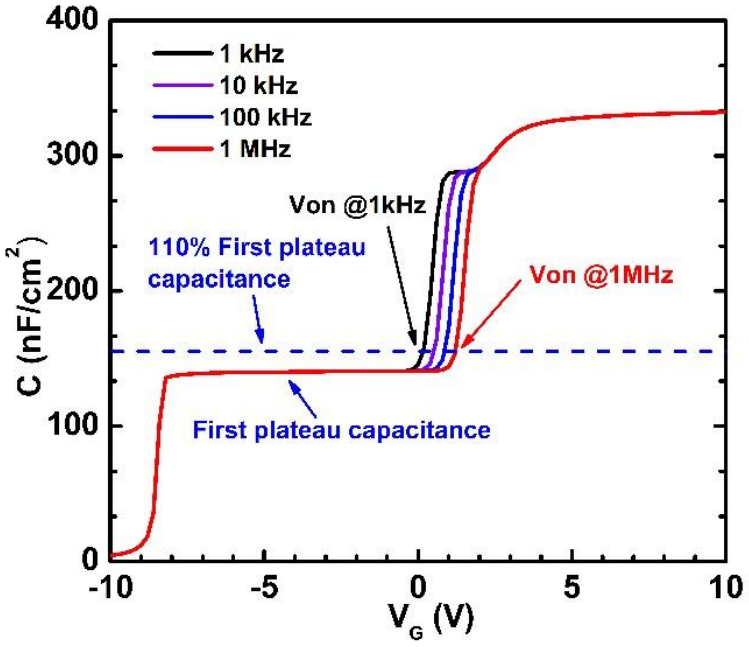


Fig. 3.18 The schematic diagram of onset voltage extraction

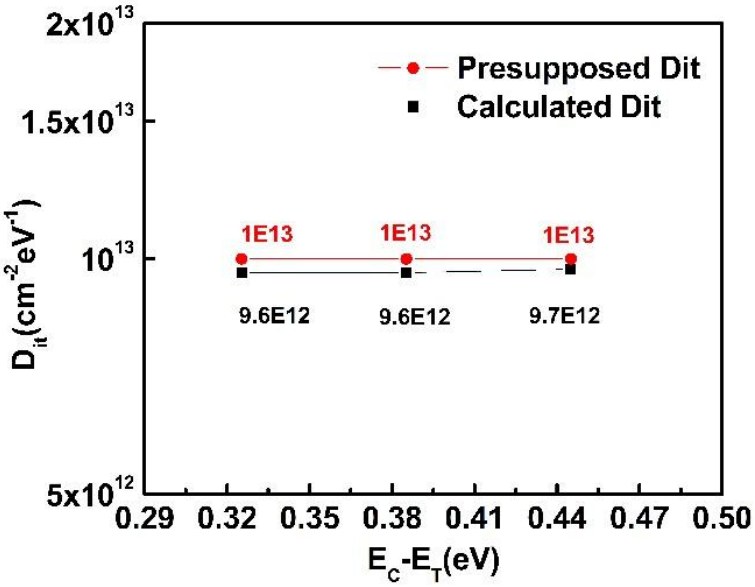


Fig. 3.19 Comparison of the presupposed D_{it} distributions in simulation and the calculated D_{it} distributions according to the simulated C-V curves.

3.6 DC I-V characterization on the GaN MIS-HEMTs

The gate dielectric breakdown characteristics of four samples are shown in Fig. 3.20. The breakdown voltage of the gate dielectric Al_2O_3 was defined at where the gate leakage current reached 1 μA/mm. It can be observed that the gate breakdown voltage of samples A, B, C and D are 10.1 V, 11.1 V, 12.5 V and 13.2 V, respectively. A breakdown electric field of 6.6 MV/cm is obtained from the O_2 plasma treated sample, which is higher than that of the other three samples. The higher breakdown electric field is attributed to the formation of a thin oxidized GaN-cap layer in the gate region. The increase of actual gate dielectric thickness can also be proved by the maximal capacitance decrease of the O_2 plasma treated MIS-capacitor. The breakdown characteristics of the ODT treated sample and the HCl treated sample are similar. It comes from the fact that the ODT treatment can finitely improve the dielectric breakdown characteristics.

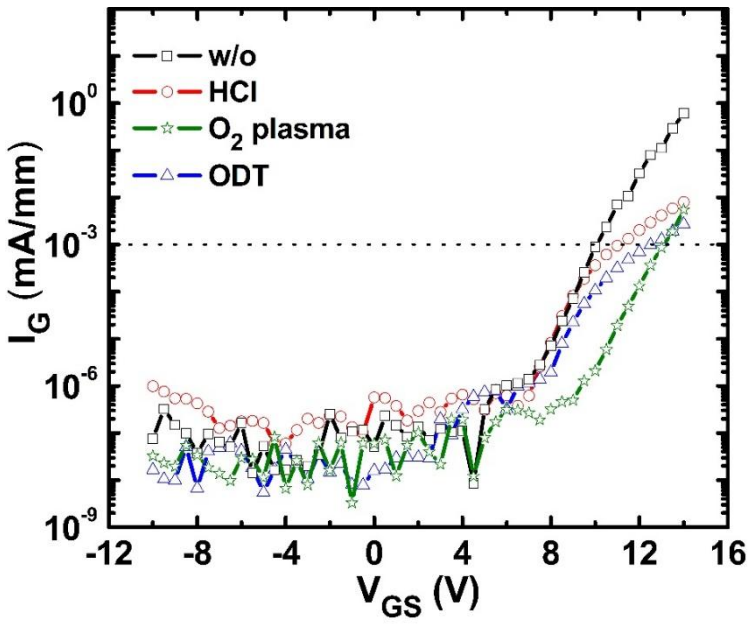


Fig. 3.20 Gate leakage current characteristics curves of the MIS-HEMTs

Fig. 3.21 shows DC transfer characteristics of the Al_2O_3/GaN/AlGaN/GaN MIS-HEMTs at V_{DS} of 10 V. The gate control characteristic of MIS-HEMTs is an important issue which can be determined from I_{DS}-V_{GS} curves near the subthreshold region. The threshold voltage (V_{th}) of samples A, B, C and D are determined to be -13.1 V, -11.8 V, -10.4 V, -12.3 V, respectively, with a drain current criterion of 1 μA/mm. Comparing with the non-treated sample, V_{th} shifted towards a positive direction for samples B, C and D likely to be due to the reduction of positive charges on the pre-treated GaN surface prior to the formation of Al_2O_3. The presence of positive charges can be explained as Ga dangling bonds on the GaN surface acting as positive charge centers, being generated due to N diffusing and leaving from Ga-N bonds [41]. A more positive V_{th} of the O_2 plasma treated sample was observed, and the reduction of positive charges indicates the O_2 plasma can passivate the N vacancies at the Al_2O_3/GaN interface effectively. The I_{ON}/I_{OFF} ratio of the four samples A, B, C and D are estimated to be ~$7x10^6$, ~$2x10^8$, ~$1x10^{10}$, ~$1x10^{10}$, respectively. For samples with the ODT and O_2 plasma treatments, the off-state leakage current was suppressed by over 3 orders as compared to the sample without treatment. It suggests that the N vacancies and impurities on the GaN surface can be reduced by using the ODT and O_2 plasma treatments, hence causing a suppressed gate-induced drain leakage effect [16]. Samples A and B exhibit a larger threshold voltage hysteresis (ΔV_{th}) of ~0.3 V and ~0.18 V, the subthreshold slope (S.S) of ~150 mV/dec and ~100 mV/dec, respectively, revealing higher interface trap density at the Al_2O_3/GaN interface. In contrast, a small threshold hysteresis (ΔV_{th}) of ~0.12 V, as well as a small subthreshold slope of ~73 mV/dec are

observed for the ODT treated sample. The latter is another evidence that the interface traps have been suppressed effectively by the ODT treatment. The O_2 plasma treated sample also exhibits a reduced ΔV_{th} of ~0.10 V and a reduced S.S of ~68 mV/dec, which are slightly smaller than that of the ODT treated sample. Among the three types of surface treatment methods, the low-cost ODT treatment has demonstrated improved gate control characteristics of associated MIS-HEMTs with an increased I_{ON}/I_{OFF} ratio, a reduced $\Delta V_{th,}$ and a reduced S.S. Although the O_2 plasma treated devices exhibited the best sub-threshold performance, as a dry process, the O_2 plasma treatment have relatively highest demands on facilities. Note that the variation of the I_D-V_{DS} curves for the four samples has not been found to be obvious. Hence the output characteristics for the samples have been excluded.

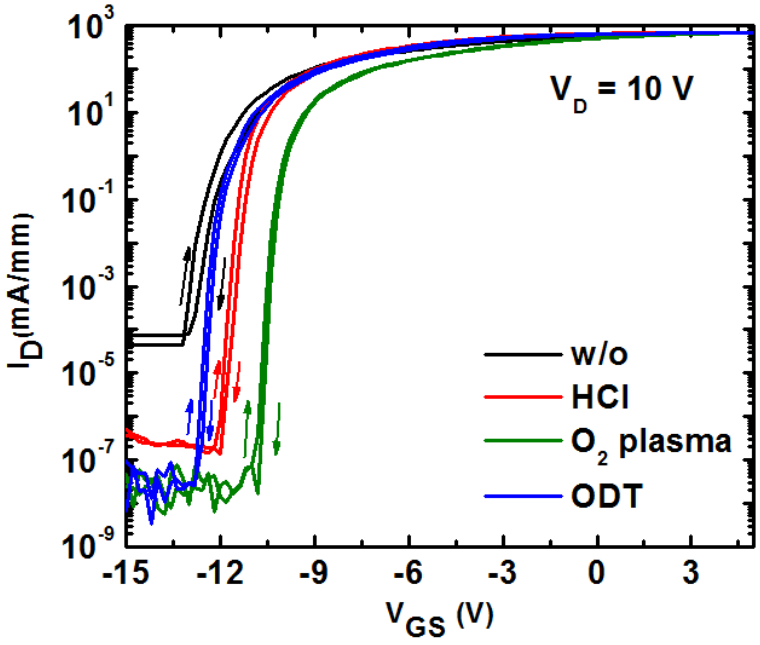


Fig. 3.21 Transfer characteristics curves of the devices at V_{DS} of 10 V in the semilog scale.

Note that, the V_{th} of the ODT treated sample shift to negative compared to HCl

and O_2 plasma treated sample is due to the more reduction of interface state density. To explain the negative V_{th} shifts, the expression formula of the V_{th} of GaN-based MIS-HEMTs needs to be analyzed. The expression formula can be found as [42]:

$$V_{th(MIS-HEMT)} = \varphi_b + \frac{Q_{p1}}{C_B} - \Delta E_{C1} - \frac{Q_{int}}{\varepsilon_{ox}} t_{ox} - \frac{q}{\varepsilon_{ox}} \int_0^{t_{ox}} x n_{ox} d_x \quad (3.11)$$

where φ_b is the barrier height at Ni/GaN interface, Q_{p1} is the resultant polarization charge at AlGaN/GaN interface, C_B is the barrier layer capacitance. ΔE_{C1} is the conduction band offset between AlGaN and GaN. Q_{int} is the total interface charge at the interface between the gate dielectric and GaN, ε_{ox} is the permittivity of the ALD-Al_2O_3, t_{ox} is the thickness of the ALD-Al_2O_3 and n_{ox} is the uniformly distributed positive charge across the gate dielectric ALD-Al_2O_3. Since the structure of the four groups of samples is identical, the gate dielectric is deposited in the same condition. The variation of Q_{int} (ΔQ_{int}) is the only element that can affect the V_{th} shift of devices. The total interface charge Q_{int} can be expressed by,

$$Q_{int} = Q_{sp2} + Q_{fn} + Q_I - qN\text{it} \quad (3.12)$$

where Q_{sp2} is the spontaneous polarization charge at GaN surface, Q_{fn} as a sheet of charge near the Al_2O_3/GaN interface, Q_I is the positive charge present at the Al_2O_3/GaN interface. Nit is the interface trap density at the Al_2O_3/GaN interface. Therefore, the variation of V_{th} (dV_{th}) can be expressed by,

$$dV_{th} = \frac{\Delta Q_{int}}{\varepsilon_{ox}} t_{ox} = \frac{\Delta Q_I - \Delta qN\text{it}}{\varepsilon_{ox}} t_{ox} \quad (3.13)$$

The dV_{th} of samples B, C and D are extracted to be 1.3 V, 2.7 V and 0.8 V, respectively. Here, the values of dV_{th} were extracted as the V_{th} of samples minus that of the non-treated sample (-13.1 V). Since the gate structure is identical for all samples, the dV_{th}

could be mainly depended on the presentation of positive charge and interface trap at Al_2O_3/GaN interface those two parts.

According to the study[18], the donor-like traps remain on their neutral charge state, independent of the bias sweeping. The charge neutrality level $E_i \approx E_C$ -1.6 eV is a demarcation point for acceptor- and donor-like interface traps. In addition, for the interface trap qNit estimation, time constants for electron emission from the interface states using the Shockley-Read-Hall statistics should be taken into account. E_{Tm} is the deepest energy of the state, which can respond the sweeping of gate signal during the I_D-V_{GS} measurement. E_{Tm} can be described by using Shockley-Read-Hall statistics as:

$$E_{Tm} = kTln(\sigma_n N_C v t_{meas}) \quad (3.14)$$

where k is the Boltzmann constant, T is the temperature, and σ is the capture cross section of the interface states, N_C is the effective density of states in the conduction band of the GaN, v is the thermal velocity of electrons and t_{meas} is the time of gate signal sweeping from -15 V to 5 V. Assuming that $\sigma_n = 1x10^{-14}$ cm^2, t_{meas} was estimated to be 1 s, E_{Tm} was estimated to be 0.8 eV from the conduction-band edge in the Al_2O_3/GaN structure. It means that only the interface traps in the energy level from E_C to E_C - 0.8 eV can be trapped or de-trapped accordingly with the gate voltage sweep. However, due to the associated long emission time constants, the deep acceptor-like interface traps in the energy level from E_C - 0.8 eV to E_C - 1.6 eV are in "frozen states", which can trap electrons during the I-V sweeping, but cannot de-trap electrons after the gate bias removal. These traps act as negatively fixed charges, which leads to a more positive V_{th} comparing with the ideal device without a D_{it} [19].

The interface state density at E_C - 0.47 eV is calculated to be 1.86×10^{13} $cm^{-2}eV^{-1}$ for sample A, 1.57×10^{13} $cm^{-2}eV^{-1}$ for sample B, 0.59×10^{13} $cm^{-2}eV^{-1}$ for sample C, and 0.37×10^{13} $cm^{-2}eV^{-1}$ for sample D by multi-frequency C-V measurement. Therefore, the difference of interface state $\Delta qN\mathrm{it}$ can be estimated as

$$\Delta qN\mathrm{it}_{AB} = (1.86\times10^{13} - 1.57\times10^{13}) \times 0.8\,eV = 2.32\times10^{12}\ \mathrm{cm}^{-2}$$

$$\Delta qN\mathrm{it}_{AC} = (1.86\times10^{13} - 0.59\times10^{13}) \times 0.8\,eV = 1.016\times10^{13}\ \mathrm{cm}^{-2}$$

$$\Delta qN\mathrm{it}_{AD} = (1.86\times10^{13} - 0.37\times10^{13}) \times 0.8\,eV = 1.192\times10^{13}\ \mathrm{cm}^{-2}$$

According to the V_{th} expression formula, a larger reduction of interface state density at the Al_2O_3/GaN interface can cause a more backward V_{th} shift. The reduction of interface state density by using the ODT is the most among the three treatments. Hence, the V_{th} of the ODT treated sample shifts to negative compared to HCI and O_2 plasma treated sample that is due to the more reduction of interface state density. In addition, when comparing with the Non-treated sample, the change in fixed charge could also be calculated as:

$$\Delta Q_{I\_AB} = \frac{\Delta \mathrm{V}_{\mathrm{th(MIS-HEMT)\_AB}} \times \varepsilon_{ox}}{t_{ox}} - \Delta qN\mathrm{it} = 4.96\times10^{12}\ \mathrm{cm}^{-2}$$

$$\Delta Q_{I\_AC} = \frac{\Delta \mathrm{V}_{\mathrm{th(MIS-HEMT)\_AC}} \times \varepsilon_{ox}}{t_{ox}} - \Delta qN\mathrm{it} = 1.56\times10^{13}\ \mathrm{cm}^{-2}$$

$$\Delta Q_{I\_AD} = \frac{\Delta \mathrm{V}_{\mathrm{th(MIS-HEMT)\_AD}} \times \varepsilon_{ox}}{t_{ox}} - \Delta qN\mathrm{it} = 1.35\times10^{13}\ \mathrm{cm}^{-2}$$

Comparing with the HCl treatment, the O_2 plasma, and the ODT treatment methods could reduce the positive fixed charge more effectively.

Moreover, in order to make a solid statement on hysteresis, S.S and breakdown characteristics, a couple of sites on each wafer had been measured to get enough statistics. The area of the GaN/AlGaN/GaN wafer is 13 mm × 13 mm for each sample,

and all of the D-mode MIS-HEMTs are located in a 1.9 um × 9 mm rectangular area. I have randomly measured the I_D-V_{GS}/I_G-V_{GS} curves of five MIS-HEMTs on each sample. These five MIS-HEMTs are with an identical structure and located in rank with a distance of over 600 um. The I_D-V_{GS}/ I_G-V_{GS} curves of the samples are plotted in Fig. 3.22. The mean value and the standard deviation of each sample have been calculated, and the error bar of the I_{ON}/I_{OFF} ratio, V_{th}, V_{th} hysteresis and S.S have also been extracted in Fig. 3.23.

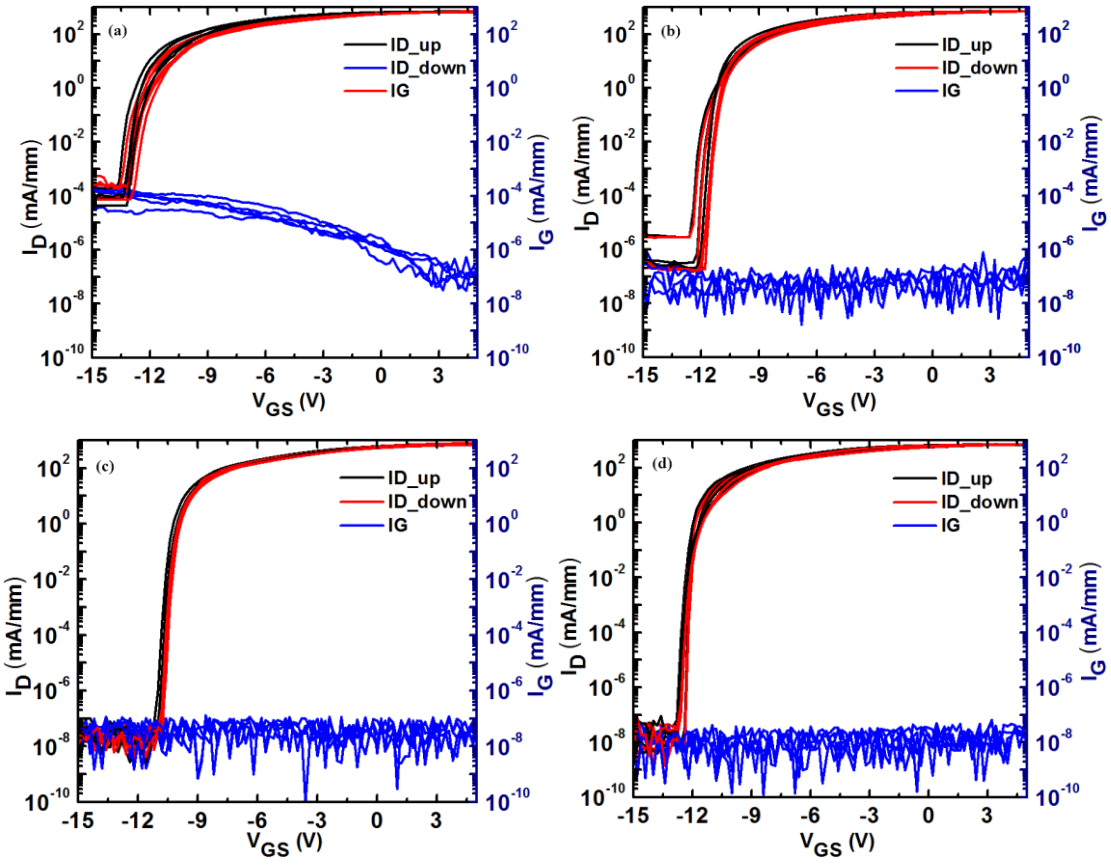


Fig. 3.22 Transfer characteristics and gate leakage current curves of (a). Non-treated (b). HCl-treated (c) O_2 plasma treated (d). ODT-treated MIS-HEMTs at a drain bias of 10 V

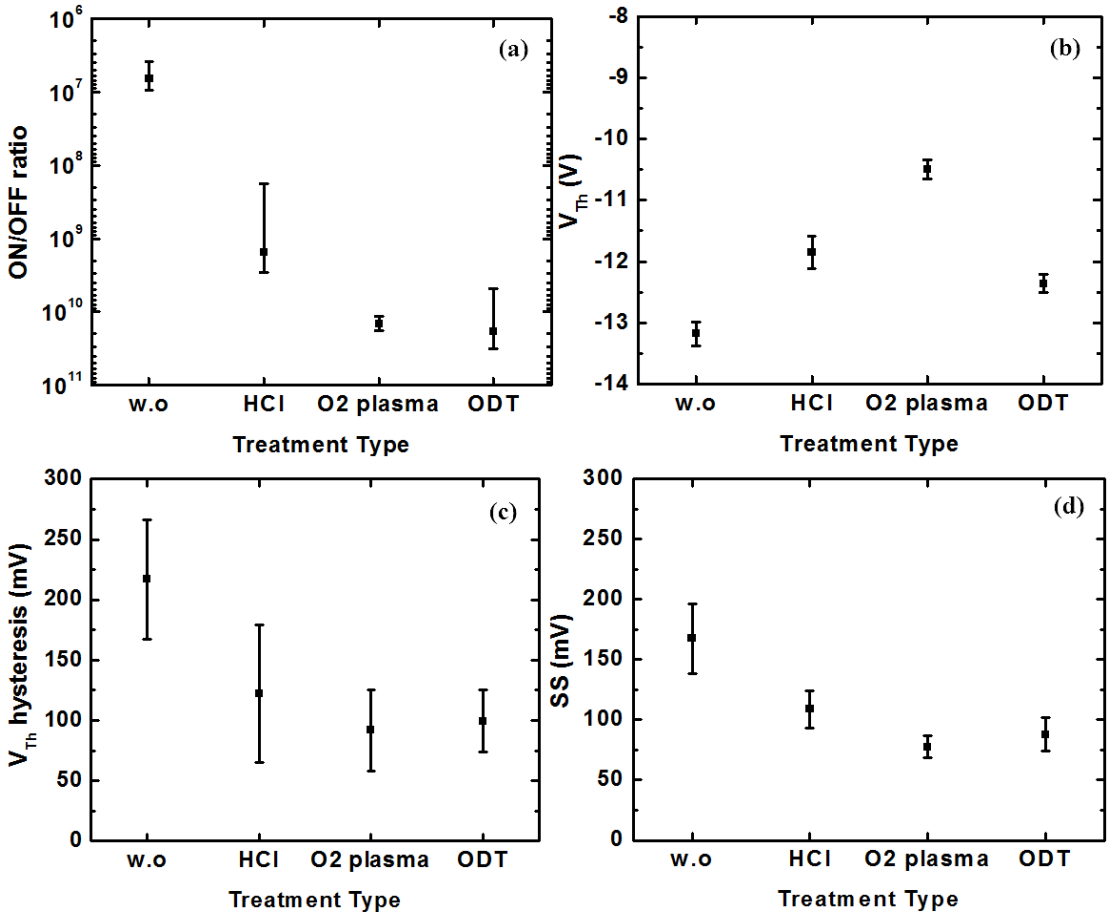


Fig. 3.23 The mean value and the standard deviation of (a) the I_{ON}/I_{OFF} ratio, (b)V_{th}, (c)Vth hysteresis and (d) S.S of each sample.

To assess V_{th} stability of the MIS-HEMTs fabricated using four types of treatments, a bias of V_{GS}= 5 V is applied to the devices, and the change of transfer characteristics was monitored. The gate bias is applied only to the gate terminal, with both drain and source grounded. With a gate bias of 5 V, the corresponding electric field in the Al_2O_3 gate dielectric layer is approximately 2.5 MV/cm. The total bias time was fixed at 21000 s. The threshold voltage shift was monitored by an I_D–V_{GS} measurement after certain bias time intervals (0, 1, 2.1, 4.6, 10, 21, 46, 100, 210, 460, 1000, 2100, 4600, 10000, and 21000 s). Fig. 3.24 shows the multiple I_D-V_{GS} curves during the 21000 s

gate bias. The positive V_{th} shift was observed for all samples after the forward bias stress. When the gate bias is sufficiently positive, the high-field regime promotes the conduction of electrons from the GaN interface through the gate dielectric to the gate metal. This phenomenon possibly leads to charge-trapping at the Al_2O_3/GaN interface, and at the pre-existing Al_2O_3 bulk traps close to the interface [43], causing detrimental effects reflected in the positive shift of V_{th}. A much larger shift of I_D–V_{GS} curves have been observed for samples A and B, while the transfer characteristic stability for sample C with O_2 plasma treatment is well behaved, as shown in Fig. 3.24(c). The shift of I_D-V_{GS} curve of sample D is larger than that of sample C after the stress time is increased.

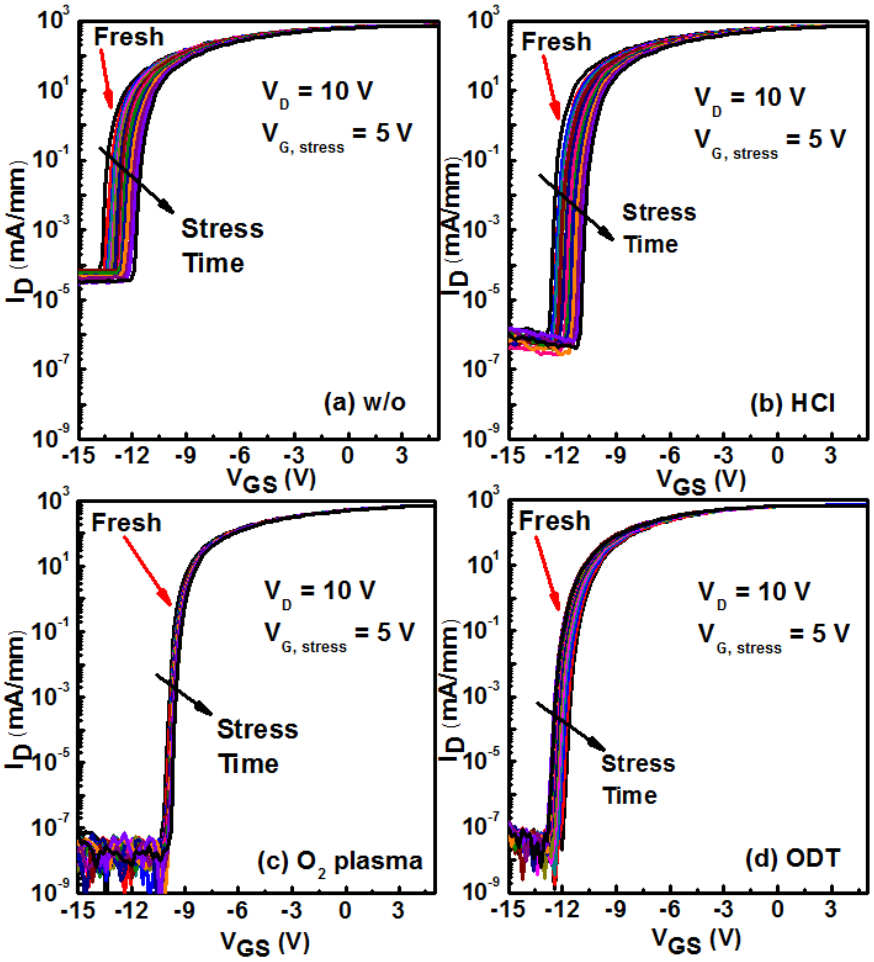


Fig. 3.24 Transfer characteristics curves measured during the 21000 s gate bias. (a) Non-treated (b) HCl treated (c) O_2 plasma treated (d) ODT treated samples of MIS-HEMTs.

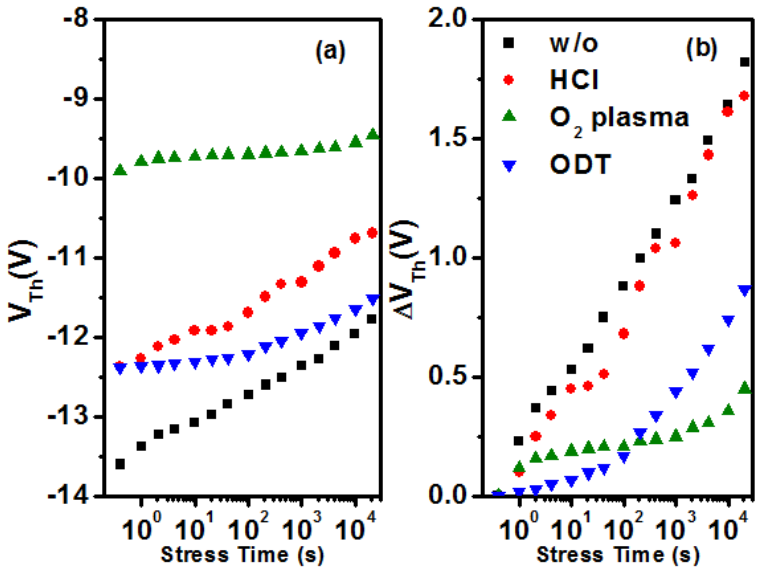


Fig. 3.25 (a) Threshold voltages measured (b) V_{th} shift during the 21000s bias for four samples.

Threshold voltages and their shifts during the 21000 s gate bias time for the four samples are shown in Fig. 3.25(a) and (b). A stress time dependent shift of V_{th} to even more positive values is observed for all samples. The V_{th} shift process consists of the initial large V_{th} shift after 1 s positive gate stress followed by a more gradual V_{th} shift when the bias time increased to 21000 s. These observations can be explained by a rapid occupation of interfacial traps occurring initially, followed by much slower tunneling of electrons to the dielectric bulk traps [44, 45]. The MIS-HEMTs with the ODT treatment show a relatively small initial V_{th} shift (~0.1 V) when compared to the other three samples. This indicates that the Al_2O_3/GaN interface trap density has been reduced significantly by the ODT treatment. In addition, the O_2 plasma treated sample shows a reduced V_{th} shift of ~0.5 V with a further increase in bias duration compared to samples A, B, and D. Since the surface treatments have a limited effect on the bulk properties of the gate dielectric, the bulk trap density is likely to be similar for all samples. The O_2 plasma treated MIS-HEMTs are more stable than the others. This can

be explained chemically in terms of the strengths of the bonds formed, which are estimated in Table 3.2 [46, 47]. All of these bonds have been detected by using XPS.

Table 3.2 The relevant bond strengths of ODT treated GaN surface

Bond	Bond Strengths (KJ/mol)
Ga-S	361
Ga-O	487
Ga-N	212
N-S	318
N-O	174

As discussed above, the O_2 plasma treatment could fill the N vacancies on the GaN surface and break the original Ga-N bond by forming a stronger bond of Ga-O. For the ODT treated sample, sulfur on GaN bonds with Ga or forms a bond with N, both of them are weaker than the Ga-O bond. However, the N-S bond is about twice bond strength as the N-O bond, thus the surface re-oxidation is slower because it will be limited by O replacing S in Ga-S. For the HCl treated and non-treated samples, the chemical bonds on the GaN surface consist of Ga-N, Ga-O, N-O and N vacancies. Note that Ga-N, N-O and N vacancies are less stable than the Ga-S or Ga-O bonds. The O_2 plasma treatment is capable of filling the N vacancies and forming a stronger bond of Ga-O. It is speculated that the O_2 plasma treated interface covered with Ga-O bonds in6y saturated, which is more stable under electrical stress. Thus, sample C exhibited a reduced V_{th} shift. To gain a better understanding of the electron transfer mechanism, the negative bias V_{th} instability measurement and the continuous recovery measurement

are required to be performed in further researches.

3.7 Summary

In this Chapter, the surface treatments prior to ALD-Al_2O_3 deposition on the GaN/AlGaN/GaN heterostructure has been investigated. An emerging GaN surface passivation process based on the ODT treatment has been proposed to improve the Al_2O_3/GaN interface quality. The GaN surface was also treated by HCl and O_2 plasma, which had also been compared. According to the XPS results, the re-oxidation is hard to avoid on the HCl treated GaN surface. In addition, the O_2 plasma treatment can fill the N vacancies on the GaN surface by oxygen atoms. Moreover, the ODT treatment can passivate N vacancies by sulphur atoms and prevent the formation of detrimental native oxide. The multi-frequency C-V results indicate that the ODT treatment reported here is a useful process to reduce the Al_2O_3/GaN interface state density. In addition, the I-V characteristics point out that the O_2 plasma treatment is capable of reducing the positive charges on the GaN surface and reduce the positive bias-induced V_{th} instability considerably. The MIS-HEMTs fabricated using the low-cost ODT GaN surface treatment have been found to exhibit effective characteristics that are highly desirable in power switching applications, such as a low V_{th} hysteresis of 0.12 V, a small S.S of 73 mV/dec, and a high I_{ON}/I_{OFF} ratio of 10^{10}. After the researches in this Chapter, two effective GaN surface methods have been discovered, and the fabricated MIS-HEMTs exhibited satisfied sub-threshold characteristics and a relative high V_{th} stability. It is

worth noting that the novelty of the work in this Chapter is at a basic level because the ODT treatment method has not been used in further studies owing to its complex procedures. Instead, the O_2 plasma surface treatment method has been widely applied in Chapters 4 and 5 for developing the GaN-based MIS-HEMTs with a high breakdown voltage and a large conduction current

3.8 References

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CHAPTER 4 High voltage AlGaN/GaN normally-on MIS-HEMTs with high-*k* dielectrics passivation

4.1 Introduction

The GaN-based MIS-HEMTs are expected to be applied in high voltage switching systems, due to their superior characteristics of high critical breakdown field, large current density, and fast switching speed. However, despite promising high-power properties of GaN-based devices, the reliability issues induced by the passivation layer under high electric field and dynamic switching are still a major concern. Most of the conventional passivation materials on MIS-HEMTs are SiO_2 or SiN_x with relatively low relative permittivity ($\varepsilon_r < 7$), wide bandgap ($E_G > 5$ eV) and high critical breakdown field ($E_f \sim 20$ MV/cm) [1, 2]. The low-pressure chemical vapor deposition (LPCVD) of SiN_x, has been investigated as the passivation of GaN-based MIS-HEMTs to exhibit decent properties (especially in dielectric breakdown and SiN_x/GaN interface) [2]. However, the degradation of ohmic contact electrodes may occur during the high temperature (> 650 ℃) deposition process. The PECVD-SiN_x grown with a faster deposition rate at a lower temperature of ~350 ℃ has also long been a common passivation layer for GaN-based MIS-HEMTs [3]. However, the exposure of the GaN surface to the plasma in the PECVD process may cause the degradation of the SiNx/GaN interface, resulting in increased density interface states and leakage currents [4]. The high-*k* materials deposited by thermal ALD have been commonly researched

as the gate dielectric in GaN-based MIS-HEMTs, for example, Al_2O_3 (relative permittivity ε_r = ~9) [5], HfO_2 (εr = ~20) [6], ZrO_2 (εr = ~30) [7], and TiO_2 (εr = ~55) [8]. Those dielectrics possessed excellent characteristics, such as free of plasma-induced damage, high film qualities, and lower deposition temperature. The research of applying high-k dielectrics as the passivation layer on the GaN-based devices has recently begun. As one of the premier investigations on the high-k passivation, the reference [9] conducted a 2-D simulation analysis of breakdown characteristics in HEMTs as a function of ε_r of the passivation layer. This study found that the off-state breakdown voltage is enhanced when ε_r is high. A similar simulation result has been published in reference [10]. This points out that high-*k* dielectrics show great potential and advantages as a choice for the passivation layer on GaN-based MIS-HEMTs. Meanwhile, there have been few experimental researches reported the high-*k* passivation layers' effect on the high voltage properties of GaN-based MIS-HEMTs. In this Chapter, a TCAD simulation of breakdown voltage and electric field profiles in MIS-HEMTs as functions of the structure of the device was performed. After the simulation analysis, the normally-on AlGaN/GaN MIS-HEMTs with different passivation layers (with/without high-k dielectric interlayer) have been fabricated. The high-*k* dielectrics, Al_2O_3 and ZrO_2 as the interlayer between GaN cap and PECVD-SiNx passivation are considered. Reduced dynamic on-resistance and improved breakdown voltage are simultaneously exhibited on the MIS-HEMTs with high-*k* dielectrics interlayer, indicating a potential of the proposed high voltage devices structure.

4.2 Simulation of AlGaN/GaN MIS-HEMTs for improving the off-state breakdown voltage

Before the design of high-voltage AlGaN/GaN MIS-HEMTs, the Sentaurus TCAD simulation was carried out to understand the relation between the device structure and the off-state breakdown performance. The device structure analyzed in this section is illustrated in Fig. 4.1. The donor density in the undoped AlGaN barrier and GaN channel layer was set as a low value of $1x10^{15}$ cm^{-3}. The gate dielectric was set as a 20 nm Al_2O_3. The gate length L_G was set as 1.5 μm, and the source-to-gate distance L_{SG} is 1.5 μm. The gate-to-drain distance, the field plate length and the relative permittivity of the passivation layer, these three parameters were set as the variables in the simulation. The surface polarization charges were assumed to be compensated by surface-state charges, and the dynamics of surface states were not considered. The gate tunneling has not been considered in this simulation, hence, the gate tunneling current was left out of consideration. Instead, the device breakdown caused by the impact ionization of carriers and the leakage current in the GaN buffer layer was concentrated on. Moreover, a high acceptor density in the GaN buffer layer of 1×10^{17} cm^{-3} has been considered because a recent study [11] reported that a high acceptor density is required to mitigate the short-channel effects. All the electric field profiles along with the AlGaN/GaN heterojunction interface on MIS-HEMTs were simulated at a gate voltage V_G of -8 V, which corresponds to an off-state.

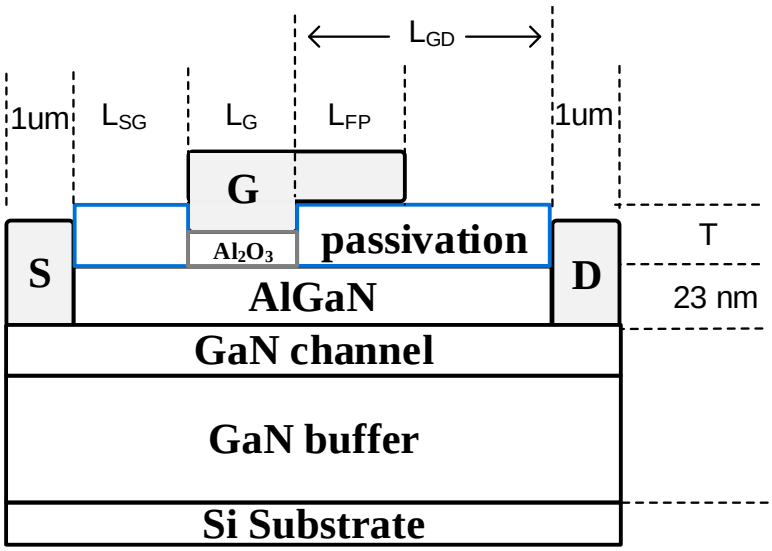

Fig. 4.1 Device structure analyzed in the 2-D simulation analysis

It is important to point out that the punch-through effects, the vertical drain-substrate conduction, the thermally activated surface leakage current, and the impact ionization are four main physical mechanisms that would cause the breakdown of HEMT devices [7]. Here, the suppression of the punch-through effects and the vertical drain-substrate conduction have not been considered in this project, because these two breakdown mechanisms were mainly dependent on the properties of the AlGaN/GaN template and the commercial AlGaN/GaN template was obtained from a company. In addition, the thermally activated surface leakage current can be suppressed by a thick and compact passivation layer, as well as a low trap density at the passivation/GaN interface. By contrast, the presence of impact ionization could be a more significant physical mechanism for the device breakdown in the actual case. It is because that the electric field is sent out from the drain electrode when a voltage applied on, and an electric field peak will be produced at the drain edge of the gate when the device is in

an off-state. The electric field at the drain-to-gate region increases as the drain voltage increases. Electrons and holes will be generated by impact ionization due to a high electric field, particularly at the drain edge of the gate. The generated charge is capable of resulting in a sudden increase in I_D and I_G, which is the cause of the direct device breakdown. Therefore, the electric field profiles along the AlGaN/GaN heterojunction interface has been extracted in order to reflect the breakdown performance of devices in this section. The comparison of the electric field profiles along the AlGaN/GaN heterojunction interface as various L_{GD} was plotted in Fig. 4.2. Here, the passivation was a 100 nm SiN_x, the field plate length (L_{FP}) was set as 0. The various L_{GD} (5 μm, 10 μm, 15 μm, 20 μm) were employed to demonstrate the effects of L_{GD} dimensions on the breakdown voltage. The electric field profiles at V_{DS} of 100 V, 200 V, 300V, 400 V and 500V were extracted. A high electric field peak was exhibited at the drain edge of the gate. It can be observed that the electric field at the drain to the gate region increases as V_{DS} increases. The increasing of the L_{GD} reduced the electric field intensity from the drain to the gate at a constant drain bias, hence the breakdown characteristics will be improved. Note that, the trade-off between the L_{GD} and breakdown voltage of GaN-based MIS-HEMTs is important because the on-state resistance of the device increases as the L_{GD} increases.

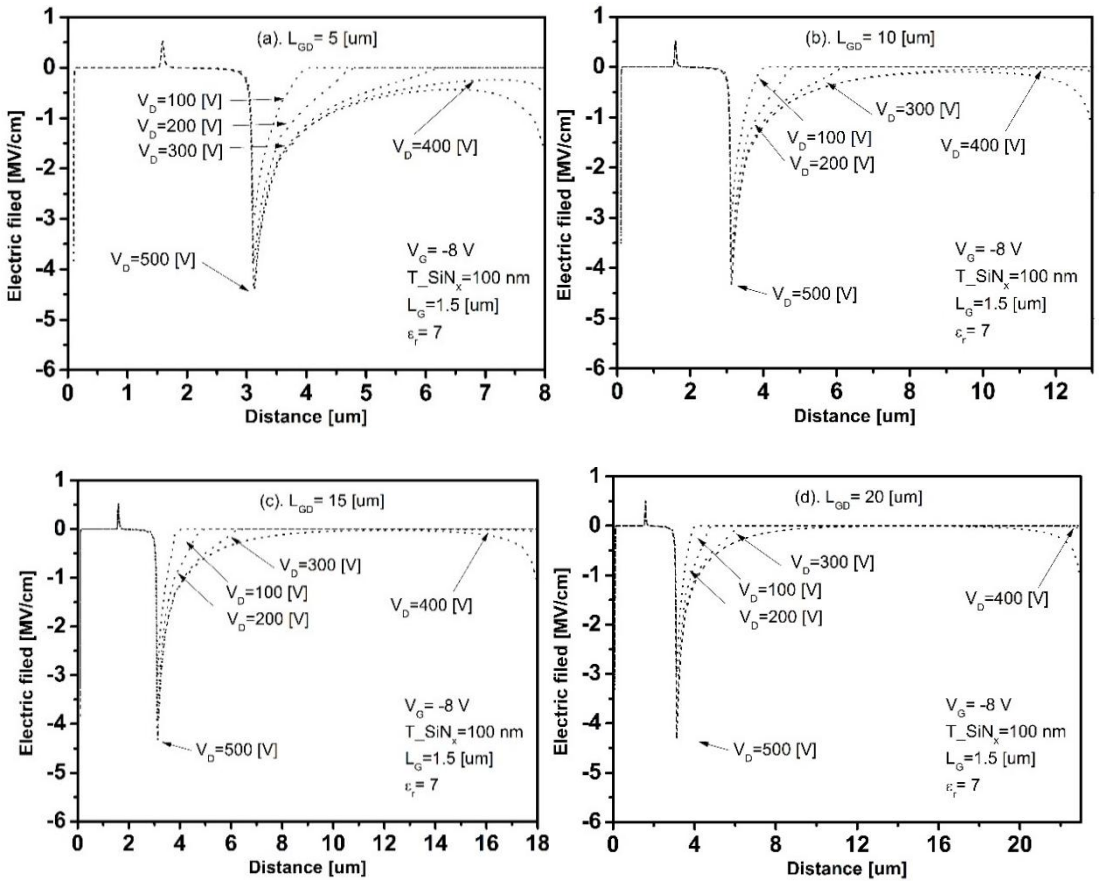

Fig. 4.2 Comparison of electric field profiles along the heterojunction interface. (a). L_{GD}= 5 μm, (b). L_{GD}= 10 μm, (c). L_{GD}= 15 μm and (d). L_{GD}= 20 μm.

Secondly, the field plate length (L_{FP}) was set as the only variable. Here, the L_{GD} was set as 5 μm. The various L_{FP} (0, 0.5 μm, 1 μm, 1.5 μm, 2 μm) were employed to demonstrate the effects of field plate length on the electric field profiles. Fig. 4.3 shows the comparison of the electric field profiles along with the AlGaN/GaN heterojunction interface when L_{FP} was set as 0 (as plotted in Fig. 4.2(a)), 0.5 um, 1 μm, 1.5 μm and 2 μm. The electric field profiles at V_{DS} of 100 V, 200 V, 300V, 400 V and 500V were extracted. It can be observed that the field plate affects the vertical electrical field underneath the gate to drain region, and the electric field peak at the drain edge of gate

is reduced significantly in each case. The field plate is capable of distributing the electric field in the channel more uniformly. On the other hand, the electric field beneath the drain region increases with the field plate length increases. A larger electric field under the drain side of the field-plate edge could cause a breakdown to occur. Note that, the employment of field plate structure has been experimentally demonstrated to improve the high voltage performance of MIS-HEMTs [12], such as the reduced current collapse and the increased breakdown voltage. Nevertheless, the field plate increases the parasitic capacitance at the same time which could cause degradation on high-frequency performance.

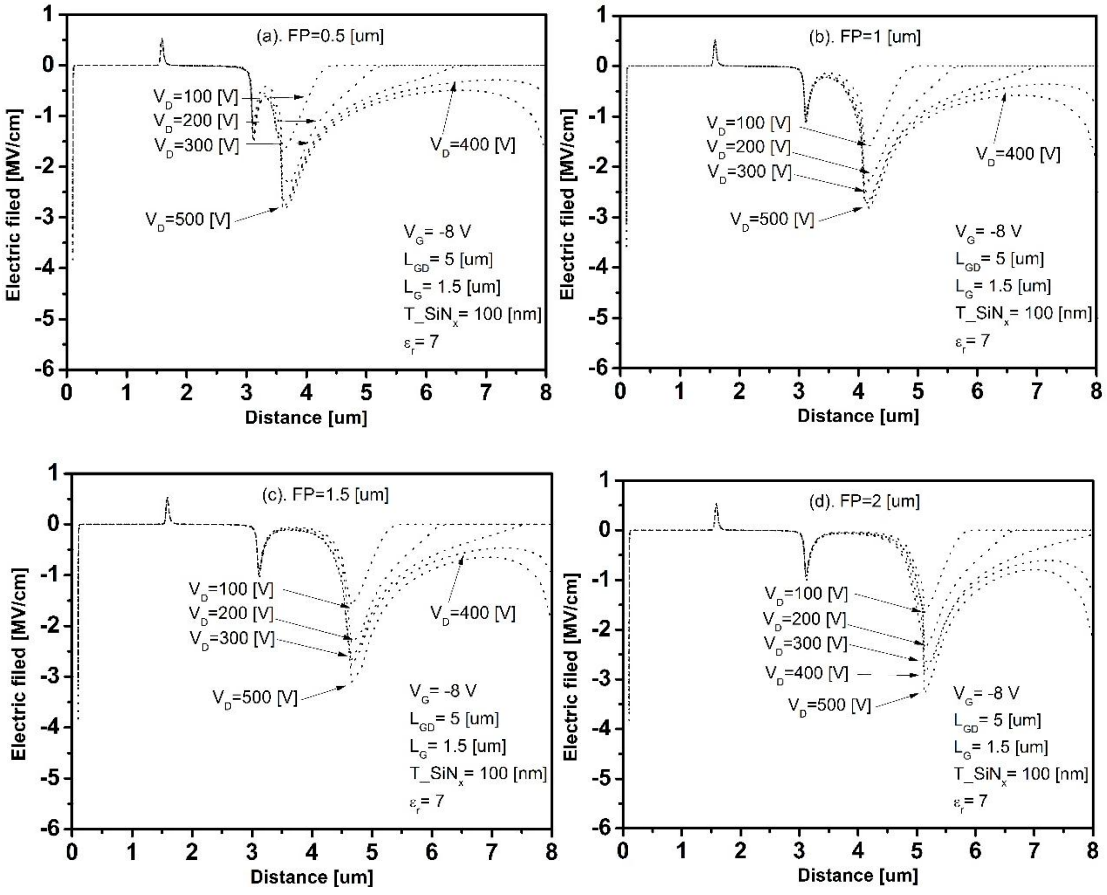

Fig. 4.3 Comparison of electric field profiles along the heterojunction interface. (a) L_{FP}= 0.5 μm, (b). L_{FP}= 1 μ m, (c) L_{FP}= 1.5 μm and (d) L_{FP}= 2 μm.

Finally, the relative permittivity of the passivation layer (ε_r) was set as the only variable. Here, the L_{GD} was set as 5 μm, the L_{FP} was set as 0 and the passivation layer was with a thickness of 100 nm. Fig. 4.4 shows a comparison of the electric field profiles along the AlGaN/GaN heterojunction interface when the ε_r was set as 4.2, 10, 20 and 30 in the simulation evaluation. The electric field profiles at V_{DS} of 100 V, 200 V, 300V, 400 V and 500V are extracted. When ε_r = 4.2 (in Fig. 4.4 (a)), the increase in V_D is entirely applied along the drain edge of the gate. By contrast, when ε_r = 30 (in Fig. 4.4 (d)), the electric field peak is reduced. The difference in an electric field can be explained by the follows: According to Gauss's law, electric displacement (D) on dielectrics satisfies the relationship of $D = \varepsilon_0 \cdot \varepsilon_r \cdot E$, where ε_0 is vacuum permittivity. The electric field E across a dielectric is inversely proportional to its relative permittivity ε_r, if a constant voltage is applied on. When the high-*k* dielectric is passivated on the semiconductor, the electric field drop along the dielectric, and the semiconductor becomes weaker from the drain to the gate. Note that, impact ionization effect caused by a high electric field particularly at the drain edge of the gate would lead to the generation of electrons and holes. The generated carriers flow to the electrodes would cause a sudden increase in gate leakage current or drain leakage current [9]. Therefore, the passivation layer with a higher ε_r can more reduce the electric field peak at the drain edge of the gate, then the improvement of gate hard breakdown voltage would become more significant. A similar phenomenon has also been reported in Ref. [10], indicating the potential of employing high-*k* dielectrics as the passivation layer on the MIS-HEMTs.

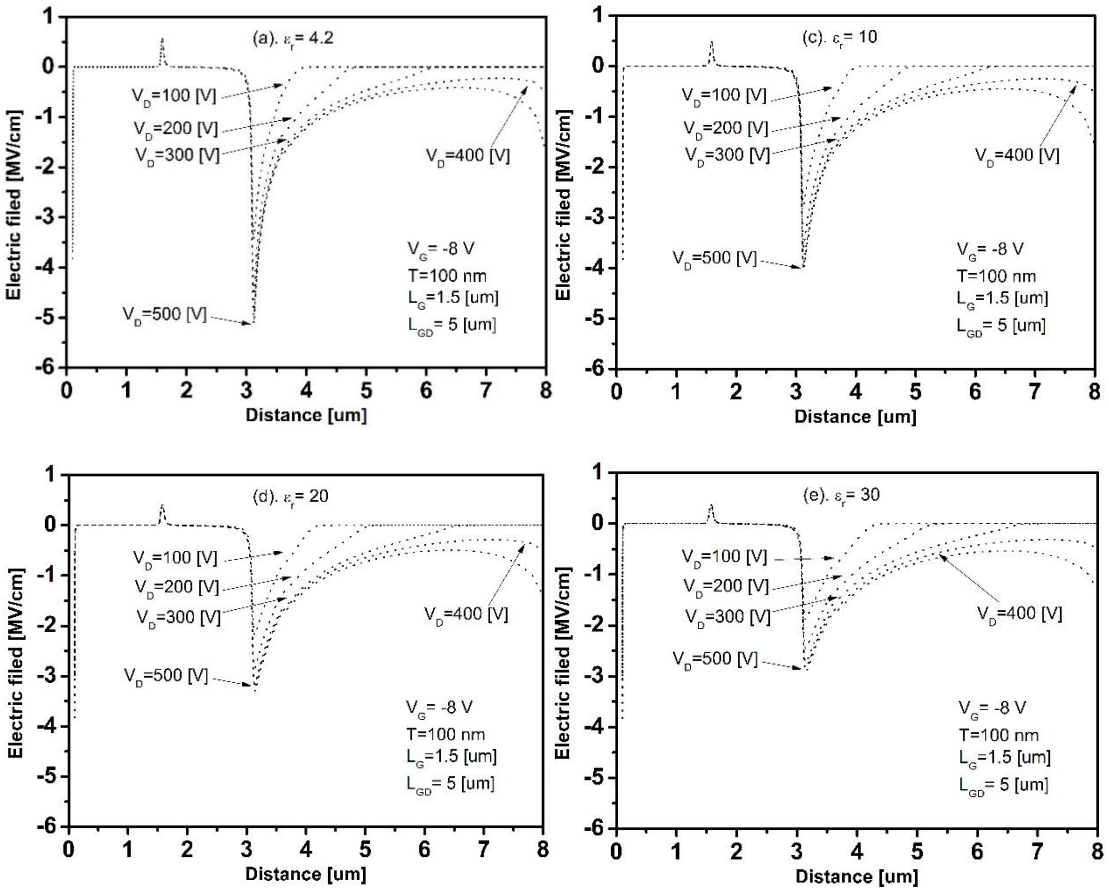

Fig. 4.4 Comparison of electric field profiles along the heterojunction interface. (a) k= 4.2, (b) k= 10 (c) k= 20 and (d) k= 30.

4.3 The detailed fabrication process of the GaN MIS-HEMTs with different passivation layers

The AlGaN/GaN MIS-HEMTs with SiN_x single-layer, with Al_2O_3/SiN_x bilayer and with ZrO_2/SiN_x bilayer passivation have been fabricated. The investigated AlGaN/GaN heterostructure epitaxial structure included from top to bottom a 2 nm thick GaN cap layer, a 22 nm undoped $Al_{0.25}Ga_{0.75}N$ barrier, a 330 nm GaN channel layer and a 5.1 μm GaN buffer on a Si substrate. The fabrication processes were started from the mesa isolation. Specifically, the mesa isolated region was formed by BCl_3/Cl_2

ICP etching. Then, Au-free source and drain electrodes were formed by electron beam evaporation of Ti/Al/Ni/TiN (30/120/55/50 nm) metal stack and followed with rapid thermal annealing at 870 ℃ in N_2 ambient for 40 s. After organic cleaning processes and a 5 mins HCl surface treatment on the wafer, a 100 nm SiN_x was deposited as the passivation for sample A. An Al_2O_3/SiN_x bilayer passivation with thicknesses of 22/100 nm was deposited for sample B. A ZrO_2/SiN_x bilayer passivation with thicknesses of 22/100 nm was deposited for sample C. The thickness of dielectrics was measured by using the spectroscopic ellipsometry. All the SiN_x was deposited by PECVD at 350 ℃ with a NH_3 flow of 10 sccm, a SiH_4 flow of 13.5 sccm, and an N_2 flow of 1000 sccm.

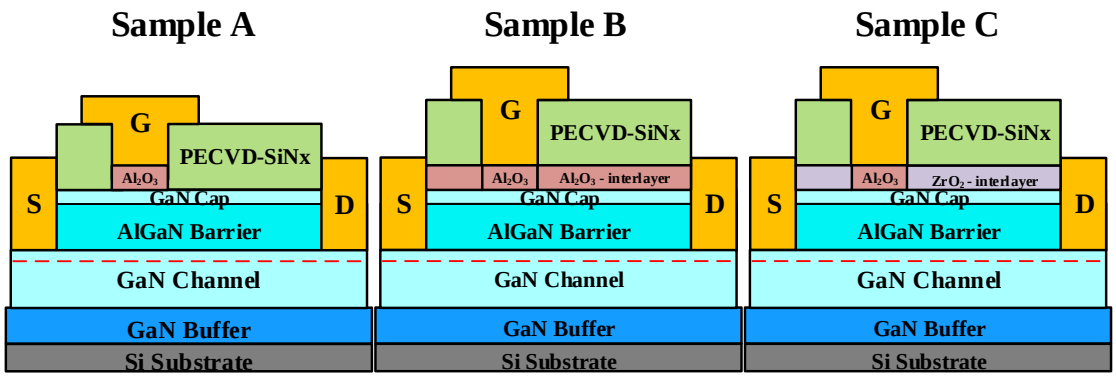

Fig. 4.5 Cross-sectional schematic view of the fabricated AlGaN/GaN MIS-HEMTs with a 100 nm SiNx single-layer passivation (Sample A), a 22/100 nm Al_2O_3/SiNx bilayer passivation (Sample B) and a 22/100 nm ZrO_2/SiNx bilayer passivation (Sample C).

The ALD-Al_2O_3 layer was grown at 230 ℃ with a growth rate of 0.11 nm/cycle. H_2O and Trimethylaluminum (TMA) were used as precursors of oxygen and Al, respectively. The ALD-ZrO_2 layer was grown at 200 ℃ with a growth rate of 0.12 nm/cycle. H_2O and Tetrakis (ethylmethylamino) zirconium were used as precursors of

oxygen and Zr, respectively. After the deposition of dielectrics, the SiN_x layer in gate regions was removed by reactive ion etching, and the Al_2O_3 and ZrO_2 layers in gate regions were etched away by 2% HF solution. A 22 nm ALD-Al_2O_3 was then deposited as the gate dielectric for three samples. Lastly, Ni/TiN (50/100 nm) metal stack was evaporated as gate electrodes followed by the pad open process. A schematic cross-sectional view of the three groups of MIS-HEMTs is demonstrated in Fig. 4.5. The fabricated MIS-HEMTs feature a fixed gate-source separation L_{SG} of 3 μm, gate length L_G of 3 μm, and gate-drain separation L_{GD} of 15 μm. The Keysight B1505A power device analyzer was used to measure the electrical properties. Transmission electron microscope (TEM) measurement has been carried out to investigate the cross-section images of the fabricated devices and the cross section TEM micrographs at the passivation region of each sample are shown in Fig. 4.6. It can be observed that the samples with the ALD dielectric interfacial layer exhibited a sharper passivation/barrier interface morphology.

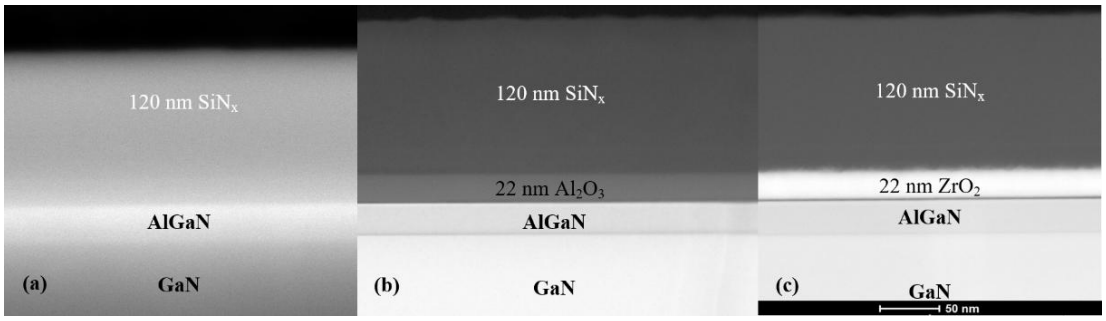

Fig. 4.6 Cross-sectional TEM micrographs at the passivation region of each sample (a) without and (b) with ALD-Al_2O_3 and (c) with ALD-ZrO_2 interfacial layer

In order to evaluate the bulk quality of the ZrO_2 thin film, a 22 nm ALD-ZrO_2 layer has been deposited on a Si substrate. The I-V and C-V measurement have been

implemented on the ZrO_2/Si MOS capacitor structure. The typical I-V curve is plotted in Fig. 4.7. It can be observed that the forward breakdown voltage of the MOS capacitor is greater than 6 V, which indicates a breakdown field of 2.7 MV/cm.

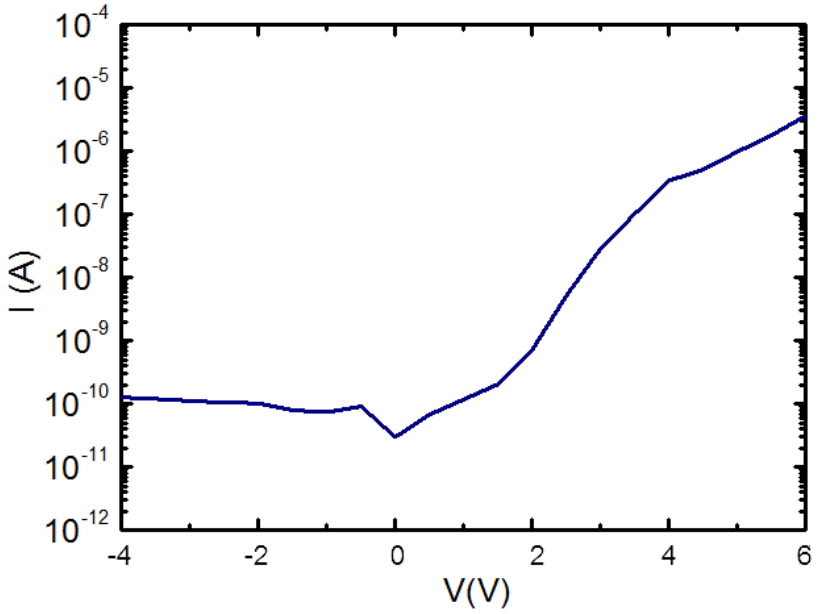

Fig. 4.7 The I-V curve of ZrO_2/Si MIS-device

The typical multi-frequency C-V curves are plotted in Fig. 4.8. The double-direction measurement gate voltage was swept from -1.5 V to 2 V with a step of 20 mV, and the frequency was varied from 100 kHz down to 4 kHz. It can be observed that the MOS capacitors exhibit a small flat-band voltage hysteresis of ~ 50 mV and a small frequency dispersion, this indicates a small density traps located at ZrO_2/Si interface and in the ZrO_2 bulk. The maximum capacitance is extracted as ~800 nF/cm^2 at 100 kHz with a forward bias of 2 V, thus the permittivity of ZrO_2 thin film was estimated as ~19.9. Note that, the permittivity of the ZrO_2 layer in this work is lower than the theoretical value (~30). Note that, the thermal ALD was used to deposit the ZrO_2 dielectrics in this study. In specific, the thin film was grown at 200 ℃, H_2O, and

Tetrakis (ethylmethylamino) zirconium were used as precursors of oxygen and Al, respectively. However, the thermal ALD technique with the H_2O oxygen source is reported to exhibiting a lower mass density due to the incorporation of OH groups into the thin film. This would result in a decrease in permittivity of dielectrics.

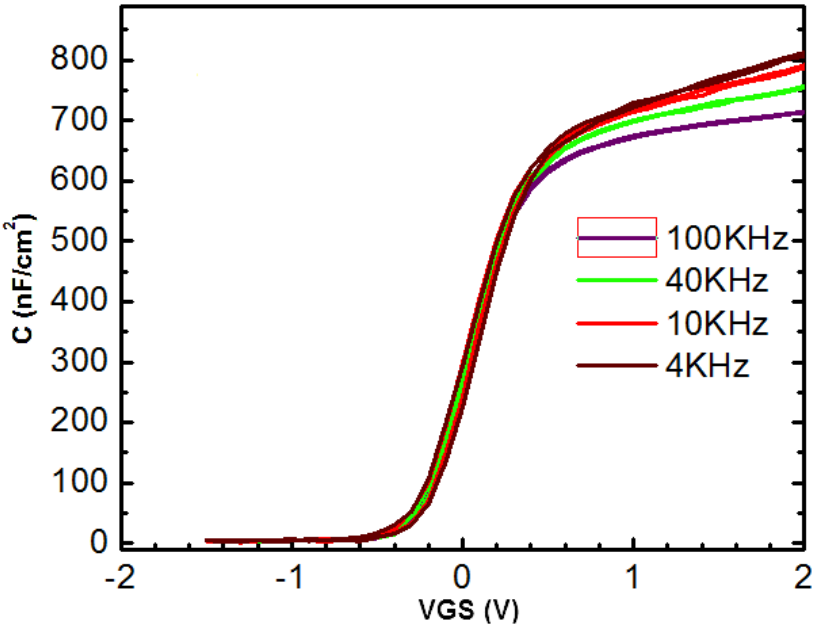

Fig. 4.8 The multi-frequency C-V curves of ZrO_2/Si MIS-device

4.4 Electrical characterization on the GaN MIS-HEMTs with different passivation layers

The DC I-V characterization on the MIS-HEMTs consists of the output and transfer characterizations, fast switching on-state resistance characterization, and off-state breakdown voltage characterization. The DC I_D-V_{DS} output curves of the MIS-HEMTs are with different passivation layers plotted in Fig. 4.9, note that the ohmic contact resistance of the devices was measured as 2.1 Ω·mm. The devices with SiN_x passivation exhibited a higher $I_{DS,max}$ of 548 mA/mm with a lower specific ON-resistance (R_{ON}) of

9.5 Ω·mm. This performance is slightly better than the MIS-HEMTs with Al_2O_3/SiNx passivation ($I_{DS,max}$ = 541 mA/mm and R_{ON} = 9.7 Ω·mm), and the MIS-HEMTs with ZrO_2/SiNx passivation ($I_{DS,max}$ = 541 mA/mm and $R_{ON,}$ = 9.7 Ω·mm).

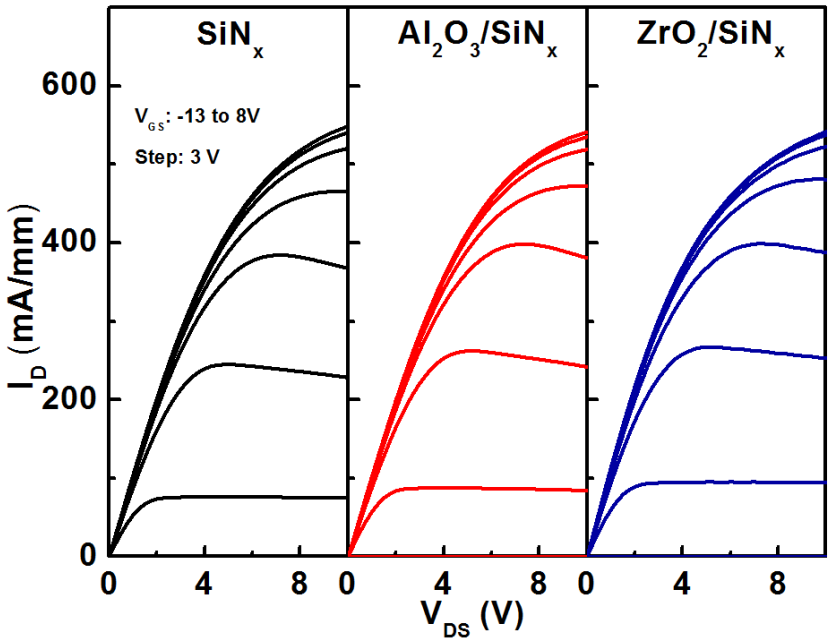

Fig. 4.9 DC I_D–V_{DS} characteristics of the AlGaN/GaN MIS-HEMTs with PECVD-SiNx passivation, Al_2O_3/SiNx passivation or ZrO_2/SiN_x passivation

The DC I_D-V_{GS} and I_G-V_{GS} curves of the three samples are plotted in Fig. 4.10. The transfer characteristics were measured by the gate voltage double-direction sweeping between -12 V and 6 V with a step of 100 m, and the drain bias was set as 10 V. The threshold voltage are extracted to be -9.6 V, -9.5 V and -9.5 V for samples A, B and C, respectively, at a drain current criterion of 1 μA/mm. Samples A, B and C exhibit a low threshold hysteresis (ΔV_{th}) of ~109 mV, ~106 mV and ~99 mV, respectively, and the subthreshold slope (SS) of ~110 mV/dec, ~101 mV/dec and ~102 mV/dec, respectively. The electrostatics characteristics (e.g. ΔV_{th} and SS) are very similar for the three samples,

because the gate structures are identical for the three devices. Moreover, the I_{ON}/I_{OFF} ratio of the three samples is calculated to be larger than $1x10^{10}$. The devices B and C with bilayer passivation are well pinched off at V_{GS} = - 12 V with an off-state drain leakage current of ~100 pA/mm, indicating the interlayer would not induce the off-state leakage currents in associated with the leakage component through mesa isolation surface [13].

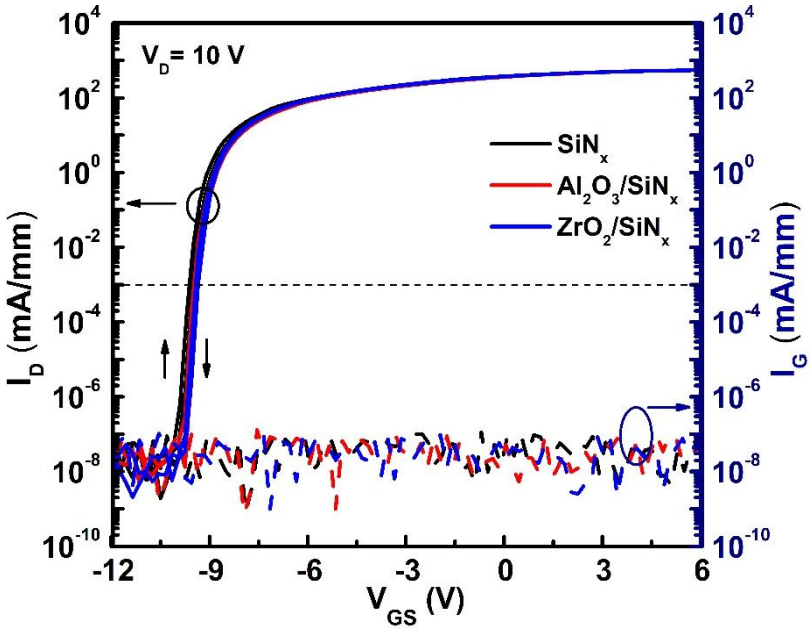

Fig. 4.10 I_D–V_{GS} and I_G-V_{GS} characteristics of the AlGaN/GaN MIS-HEMTs with PECVD-SiNx passivation (in black lines), Al_2O_3/SiN_x passivation (in red lines) or ZrO_2/SiN_x passivation (in blue lines).

The dynamic on-state performance of the three samples was evaluated by using a pulsed I_D-V_{DS} measurement under fast switching with different quiescent bias points. The schematic timings of drain and gate signals in the pulse I_D-V_{DS} measurements are demonstrated in Fig. 4.11 [14]. At the off-state, quiescent gate bias ($V_{GS, Q}$) was fixed

at -15 V and quiescent drain biases ($V_{DS, Q}$) were set as 50 V, 75 V, 100 V, 125 V and 150 V. The off-state stress time was 2 s. The pulsed output curves were measured at 500 μs after off-state voltage stresses. The on-state was chosen to feature V_{GS} = 6 V. Fig. 4.12 shows the DC and pulsed I_D-V_{DS} curves of the three MIS-HEMTs. The DC I_D-V_{DS} curves before the stresses are used as references (solid lines in black). Here, effective suppression of the current collapse by using the Al_2O_3/SiN_x passivation is demonstrated, which exhibited a small difference between the DC and pulsed output curves. Compared with the PECVD-SiN_x passivation, the ALD-dielectrics/SiN_x shows an enhanced dynamic performance with $V_{DS,Q}$ higher than 50 V.

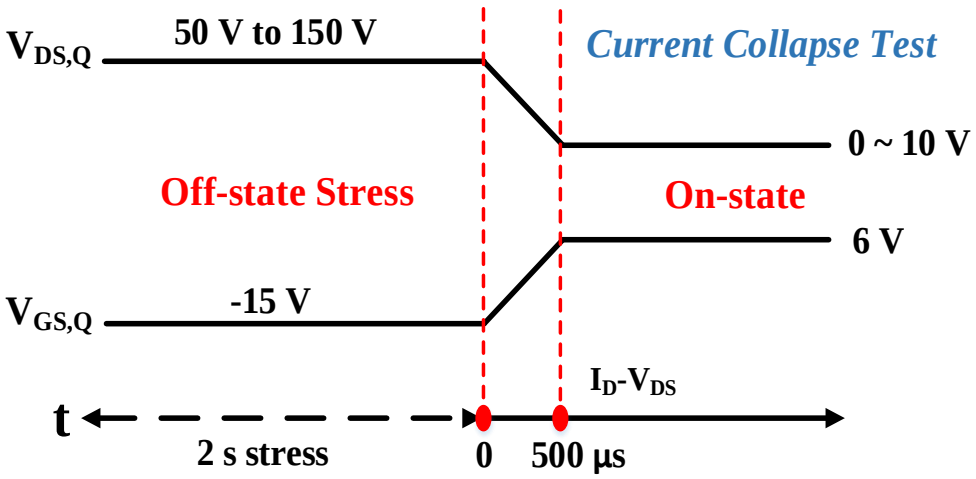

Fig. 4.11 Parameters and timings setting in current collapse measurements. Pulsed I_D-V_{DS} curves were measured at 500 μs after removing the 2 s stress bias.

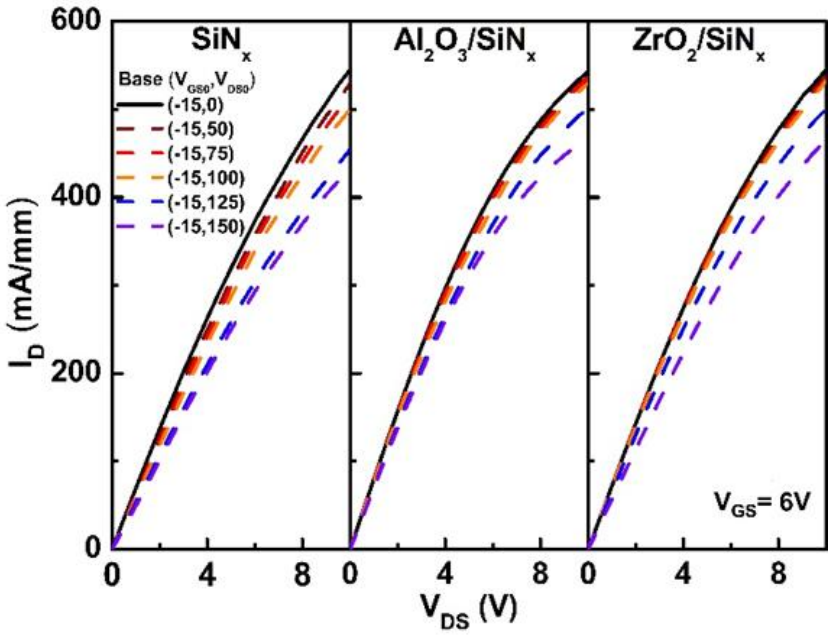

Fig. 4.12 Behavior of pulsed I_D-V_{DS} curves of the AlGaN/GaN MIS-HEMTs with different passivation layers measured at different quiescent bias points.

The degradation of dynamic on-resistance was evaluated as the ratio of dynamic on-resistance to the static on-resistance ($R_{ON,D}/R_{ON,S}$). The $R_{ON,D}/R_{ON,S}$ at different quiescent bias points of three samples are extracted and plotted in Fig. 4.13. On-state resistance was extracted from the linear region of the output curve, and it was chosen to feature V_{GS} = 6 V and V_{DS} = 0.5 V. A sharp increase of the dynamic R_{ON} is observed for the PECVD-SiN_x passivated MIS-HEMTs. Specifically, shown as the black line in Fig. 4.12, the dynamic R_{ON} of the SiN_x is 1.36 times the static R_{ON} when the off-state stress $V_{DS,Q}$ is higher than 150 V. By comparison, the dynamic R_{ON} of the Al_2O_3/SiN_x and ZrO_2/SiN_x passivated devices are only 1.14 and 1.25 times the static R_{ON} after off-state $V_{DS,Q}$ stress of 150 V, respectively. The results point out that the current collapse phenomenon could be suppressed effectively by using the high quality ALD high-*k*

dielectric as the passivation layer. The larger current collapse exhibited in the PECVD-SiN_x passivated sample is possibly caused by the plasma damage at the GaN surface during the SiN_x deposition [15, 16].

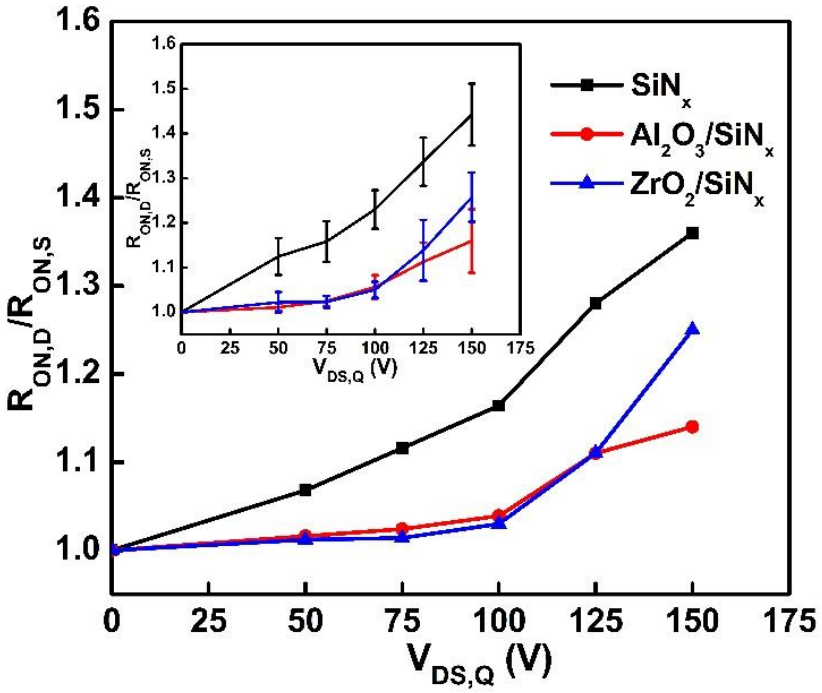

Fig. 4.13 $R_{ON,\,D}/R_{ON,\,S}$ of the fabricated AlGaN/GaN MIS-HEMTs at different quiescent drain bias points. (Inset figure: The means value and the standard deviation of $R_{ON,\,D}/R_{ON,\,S}$ at different quiescent drain bias points)

As discussed in Chapter 3, the GaN-based MIS-HEMTs are known to have a high density of states (~10^{13} $cm^{-2}eV^{-1}$) at the GaN-based surface/gate dielectric interface and the GaN-based surface/passivation layer interface. The interface traps are originated from N vacancy and native oxide on the GaN-based surface [17] as well as the plasma induced damages during the dielectric deposition or dry etching process [15]. A high density of GaN-based surface/gate dielectric interface states could result in worse electrostatics characteristics and the V_{th} instabilities, which have been demonstrated in

Chapter 3. In contrast, a high density of GaN-based surface/passivation interface states acts as the primary source of influence on 2DEG conductivity and dynamic performances of the GaN-based MIS-HEMTs [18]. Under the static state or on-state, the shallow traps at the GaN surface/passivation interface are empty owing to the strong polarization-induced electric field inside of the AlGaN barrier layer as well as a low electric field from the gate to the drain side. The schematics of charge locations in the steady state MIS-HEMTs are shown in Fig. 4.14.

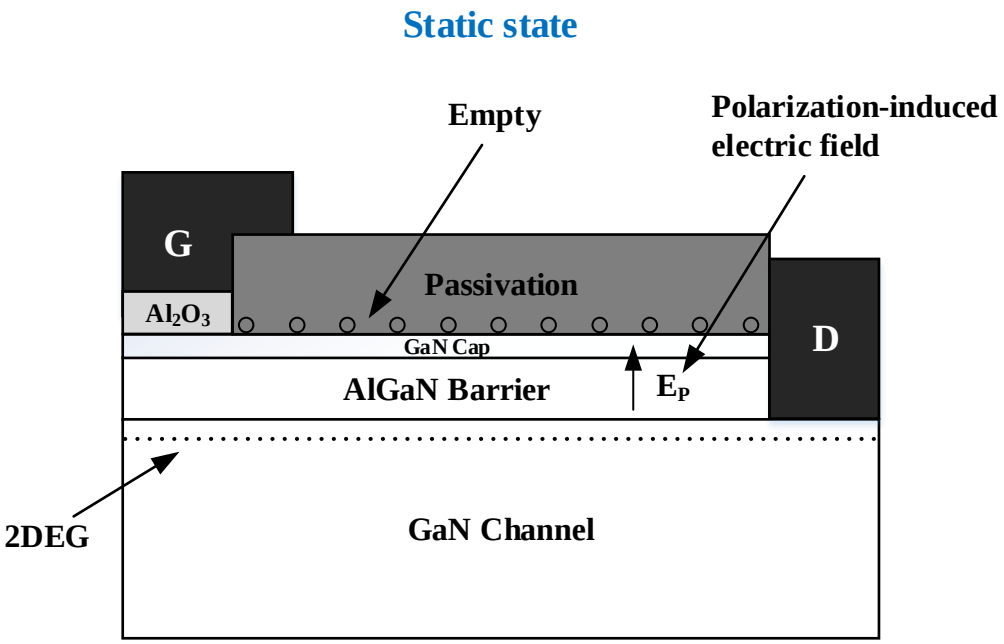

Fig. 4.14 The schematics of charge locations in the steady state MIS-HEMTs

At the off-state ($V_{GS}< V_{th}$) with high drain voltage stresses, electrons injected from the gate electrode due to a high electric field emitted from the drain to the gate direction. A number of electrons could be temporally captured by the empty acceptor states at the GaN-based surface/passivation interface. The trapped electrons induce an additional electric field to repel the electrons in the 2DEG channel and results in a reduction of

2DEG density. The schematics of charge locations in the high drain voltage stress MIS-HEMTs are shown in Fig. 4.15. In the real case, when the MIS-HEMTs is fastly switching from the off-state to the on-state, the electrons start to de-trap from the interface traps due to the reduced electric field. However, a small number of electrons are still trapped if the switching interval is short than the trap emission time. This would cause an increased dynamic on-state resistance and a reduced drain current density. Note that, for a constant state density at GaN-based surface/passivation interface, a higher drain voltage stress can result in a more electron trapping process, thus a more significant current collapse effect. Moreover, a fast switching can lead to a less electron de-trapping process before the R_{ON} measurement, thus also a more significant current collapse effect.

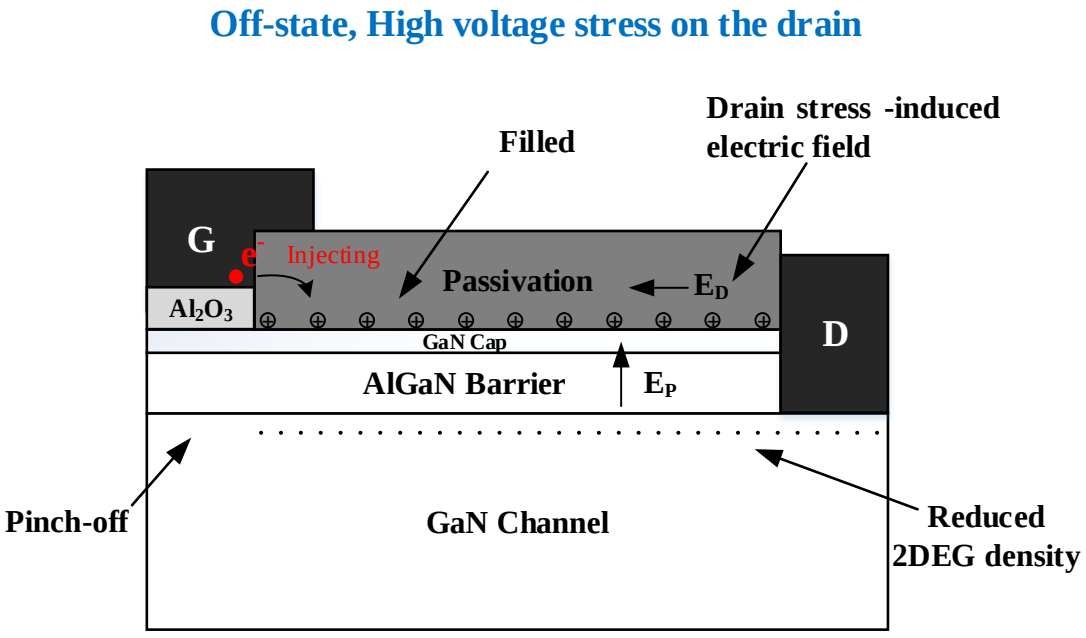

Fig. 4.15 The schematics of charge locations in the high drain voltage stress MIS-HEMTs

Using a proper passivation layer with a good interface quality toward GaN (AlGaN)

barrier surface is a feasible method to reduce the current collapse effect. The current collapse ratio of GaN-based MIS-HEMTs with different passivation layers have been compared, and the state-of-the-art results are summarized as shown in Table 4.1. It can be observed that the measured result of the Al_2O_3 sample in this study could be a fair value compared with the results in other mainstream studies.

Table 4.1 A summary of $R_{ON,S}$ / $R_{ON,D}$ ratios at 150 V drain bias for the GaN-based MIS-HEMTs from this work and the state-of-the-art literature.

Reference	Year	Passivation	Deposition technique	$R_{ON,S}$ / $R_{ON,D}$ (@ 150 V drain bias)
[19]	2013	AlN	PEALD	~1.2
[20]	2016	AlN	PEALD	~1.1
[2]	2016	SiNx	LPCVD	~1.17
[21]	2017	SiNx	PECVD	~1.7
[13]	2017	SiON	PECVD	~1.15
[22]	2019	NiO_x	Oxidation	~1.06
[23]	2019	$HfSiO_x$	ALD	~1.3
[24]	2018	SiN_x	LPCVD	~1.25
[25]	2014	Al_2O_3	PEALD	~1.25
This work		Al_2O_3	ALD	1.14
This work		ZrO_2	ALD	1.25

The MIS-capacitors with PECVD-SiN_x, ALD-Al_2O_3 or ALD-ZrO_2 as the dielectric have been fabricated to extract the shallow interface state density between the PECVD-SiNx/GaN or between the ALD-oxides/GaN. The thickness of dielectrics is 22

nm for all samples, and a 5 mins HCl surface treatment was carried out on the GaN cap layer before the dielectrics deposition. Multi-frequency C-V characteristic curves of MIS-capacitors are shown in Fig. 4.16. The measurement gate bias was swept from -10 V to 5 V with a step of 50 mV, the frequency was varied from 2 MHz down to 1 kHz, and the measurement temperature is 25 ℃. A large bias voltage could act as electric stress on the gate that would generate more defects at the dielectric/GaN interface and the bulk of the dielectric [26]. Therefore, the maximum gate bias was set as 5 V for the CV measurement to estimate the as-grown interface defects, and the detailed reasons have been discussed in Chapter 3. The C-V curves feature two rising edges. The first rising edge at negative V_G corresponds to the formation of the two-dimensional electron gas (2DEG) channel, and the second rising edge at positive V_{GS} refers to the spill-over of the 2DEG at the dielectric/GaN interface. The frequency dispersion at the second rising edge has been observed in all samples and a more significant frequency dispersion indicates a higher dielectric/GaN interface traps density. Furthermore, when applying a higher gate voltage, electrons start to be accumulated in the AlGaN barrier, leading to an increase of capacitance to the insulator capacitance. Note that the capacitance of the ZrO_2/GaN sample is higher than that of the other two samples, which is due to a higher relative permittivity of the ZrO_2 film. The obvious frequency dispersion is detected at the second rising edge for the SiN_x/GaN and ZrO_2/GaN samples. In the case of SiN_x/GaN device, the interface includes very high interface trap density (D_{it}), hence the second step at low frequency cannot be observed even at high forward gate bias [17]. By contrast, a rising edge with a smaller frequency dispersion

is observed by using the Al_2O_3 as the dielectric. The dielectrics/GaN D_{it} can be calculated by the second slope onset voltage in the multi-frequency C-V curves.

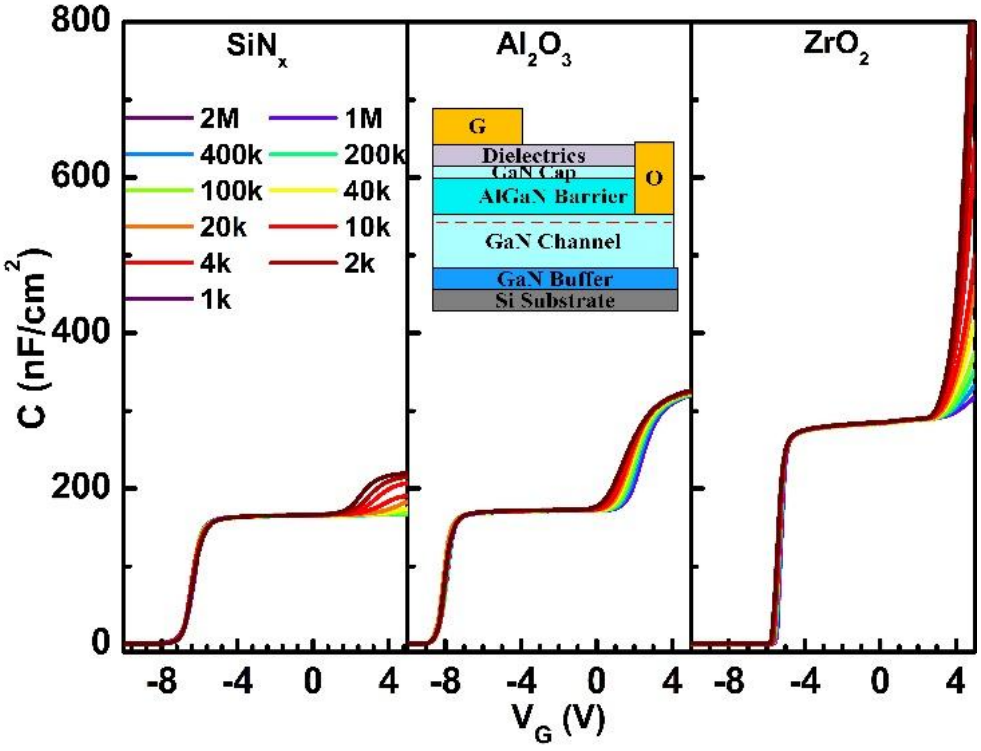

Fig. 4.16 Multi-frequency C-V characteristics of insulators/GaN/AlGaN/GaN MIS-capacitors structures with the SiN_x, Al_2O_3 and ZrO_2 as the gate dielectric. (Inset figure: cross-sectional schematic of MIS-capacitors with a 22 nm dielectric)

The C-V measurements on insulator/GaN/AlGaN/GaN MIS-capacitors with SiN_x, Al_2O_3 and ZrO_2 gate dielectrics have been carried out to compare the hysteresis. The double-direction C-V curves of MIS-capacitors are plotted in Fig. 4.17. The measurement gate bias was up-swept from -10 V to 5 V (lines in black), and down-swept from 5 V to -10 V (lines in red) with a step of 50 mV, and the ac signal frequency was set as 1 kHz. The voltage hysteresis (ΔV) are extracted in the C-V slope at the reverse bias, and the ΔV is estimated to be 150 mV, 190 mV and 370 mV for samples

A, B, and C, respectively.

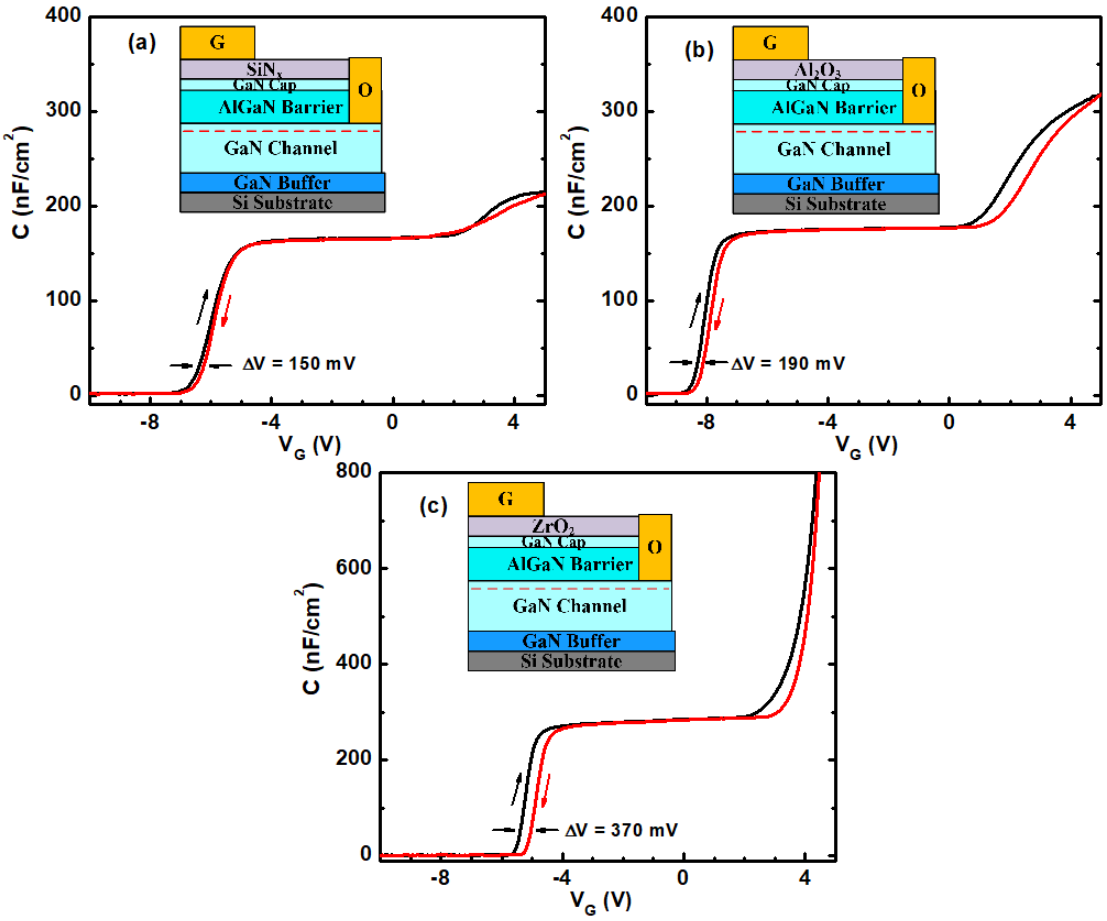

Fig. 4.17 Double-direction C-V characteristics curves of insulators/GaN/AlGaN/GaN MIS-capacitors (a) with the SiN_x, (b) with Al_2O_3 and (c) with ZrO_2 as the dielectric.

For the case with the Al_2O_3 gate dielectric, the maximum capacitance was extracted as 326 nF/cm^2, and the total capacitance (the first C-V plateau) was extracted as 174 nF/cm^2 from the Fig. 4.17(b). Note that, the second accumulation capacitance on the Al_2O_3 sample was observed. The dielectric constant of the Al_2O_3 films in this study was estimated as 8.1, which is slightly lower than its theoretical value (~9). For the case with SiN_x gate dielectric, the total capacitance was extracted as 166 nF/cm^2, which is

lower than that of the Al_2O_3 sample, indicating the difference in the dielectric constant of two films. On the other hand, the maximum capacitance of the SiN_x sample was extracted as 221 nF/cm^2. If using the maximum capacitance value to estimate the dielectric constant of the SiN_x film, the result would be 5.4 that is significantly lower than its theoretical value (~7.5). Moreover, the down-sweep C-V curve as shown in Fig. 4.17 (a) (line in red) exhibited a much steeper slope at the forward bias. It is speculated that the accumulation capacitance C_{SiNx} (or the second C-V step) was not reached in the SiN_x sample, due to a high density of traps (D_{it}) at the PECVD-SiN_x/GaN interface. Moreover, sample C with ZrO_2 dielectric exhibited a significant leakage current (> 0.1 μA/mm) at a forward bias of 5 V, the accumulation C-V plateau at forward biases were also not shown up.

Fig. 4.18 shows the interface trap density distributions at the dielectrics/GaN interface for the MIS-capacitor structures obtained from the interface state density - energy level mapping method [27]. The means value and the standard deviation of interface trap density were plotted in the inserted figure that was extracted from 8 representative devices for each sample. It is worth noting that in the D_{it} calculation, the capacitance of Al_2O_3 thin film was extracted from the Al_2O_3/GaN/AlGaN/GaN capacitor structure, and the capacitance of SiN_x, and ZrO_2 thin films were extracted from the SiN_x/Si and ZrO_2/Si MOS capacitor structures. For the SiN_x/GaN sample, the D_{it} is calculated to be over 3×10^{13} cm^{-2}eV^{-1} in the energy level range of ~0.38 eV to ~0.47 eV from the conduction band, which can be explained by the plasma damage on the exposed GaN surface during the SiN_x deposition. Moreover, the D_{it} at the shallower

energy level cannot be calculated by the C-V method, because the second steps at low frequency have not been observed. For the ZrO_2/GaN sample, D_{it} varies from 9.4×10^{12} $cm^{-2}eV^{-1}$ to 4.7×10^{13} $cm^{-2}eV^{-1}$, when the energy level depth changes from ~0.28 eV to ~0.47 eV. In comparison, the Al_2O_3/GaN sample shows the lowest D_{it} distribution among the three samples in the energy level from 1.3×10^{13} $cm^{-2}eV^{-1}$ down to 8.6×10^{12} $cm^{-2}eV^{-1}$. It demonstrates that the shallow traps on the GaN surface have been effectively suppressed by the ALD-Al_2O_3. Lower D_{it} at the dielectrics/GaN interface would have a weak electron trapping effect under quiescent stress. This also supports the suppression of the current collapse effect in the Al_2O_3/SiN_x passivated devices, as illustrated in Fig. 4.13.

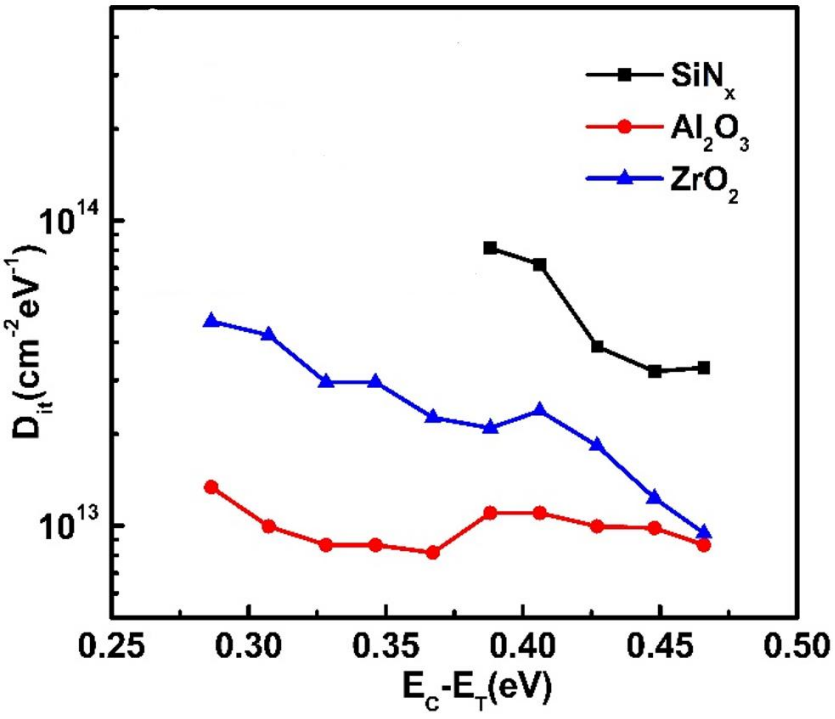

Fig. 4.18 Distribution of D_{it} vs (E_C – E_T) at the dielectrics/GaN interface extracted from C-V characteristics.

The following discussion will be focused on the development of high voltage AlGaN/GaN MIS-HEMTs and comparing the performance of the devices with different passivation structures. It is worth noting that the improvement in the breakdown voltage of AlGaN/GaN MIS-HEMTs is a 3-year work in this project. The off-state breakdown voltage of the early stage devices with PECVD-SiN_x passivation was lower than 400 V. After several attempts on improving the SiN_x film quality, the breakdown voltage of the SiN_x passivated MIS-HEMTs had been improved to ~ 700 V (as shown in Fig. 4.19, line in black). However, the devices were still not suitable for high voltage (over 1000 V) applications. This motivated me to inset a robust ALD-oxides beneath the PECVD-SiN_x passivation to further improve the breakdown performance of AlGaN/GaN MIS-HEMTs.

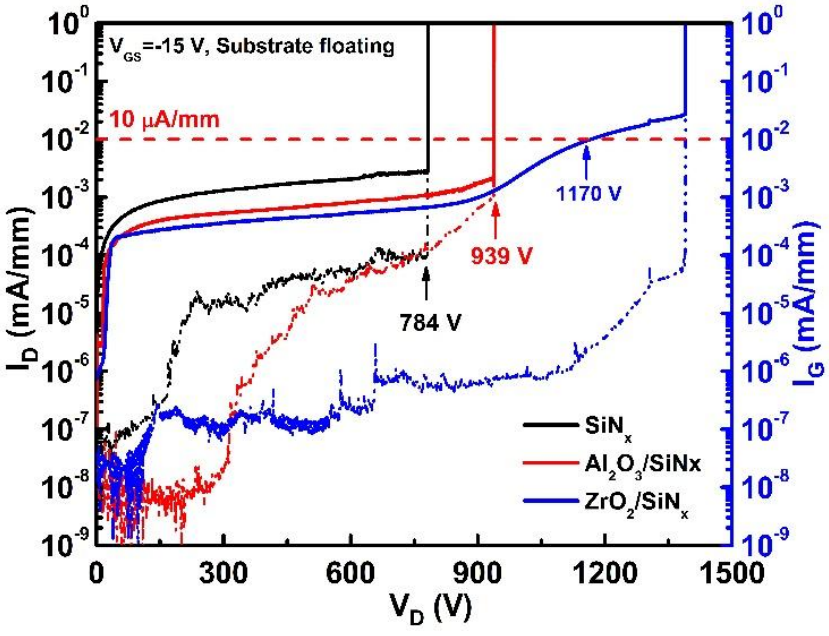

Fig. 4.19 Off-state breakdown characteristics of the fabricated AlGaN/GaN MIS-HEMTs with PECVD-SiN_x passivation (lines in black), Al_2O_3/SiN_x passivation (lines in red) or ZrO_2/SiN_x passivation (lines in blue).

Fig. 4.19 demonstrates the off-state breakdown characteristics of MIS-HEMTs with or without the inter-passivation layer at V_{GS} = -15 V with the floating substrate. Sample A passivated by PECVD-SiN_x presents a breakdown voltage of 784 V. For samples B and C with Al_2O_3 or ZrO_2 interlayer, higher breakdown voltages of 939 V and 1170 V have been extracted at drain leakage current criterion of 10 uA/mm, respectively, indicating an improved breakdown performance. Note that, the drain leakage currents were all larger than the gate leakage currents for all samples before the devices breakdown occurred. The sample with SiN_x single-layer passivation exhibited the larger off-state leakage current and ~2 order of magnitude larger leakage currents between two isolated devices compared with the other two samples. However, in further study, it is noticed that the off-state leakage current in I_G-V_{GS} curves and leakage currents between two isolated devices can be suppressed by etching outside of the mesa isolated region deeper. Moreover, the drain leakage currents became equal to the gate leakage currents on the breakdown voltage measurement for all samples. This is most probably because the GaN channel layer still existed after the insufficient mesa isolation process. Therefore, all the devices have been re-fabricated with a deeper mesa isolation etching, and the other fabrication processes remained the same.

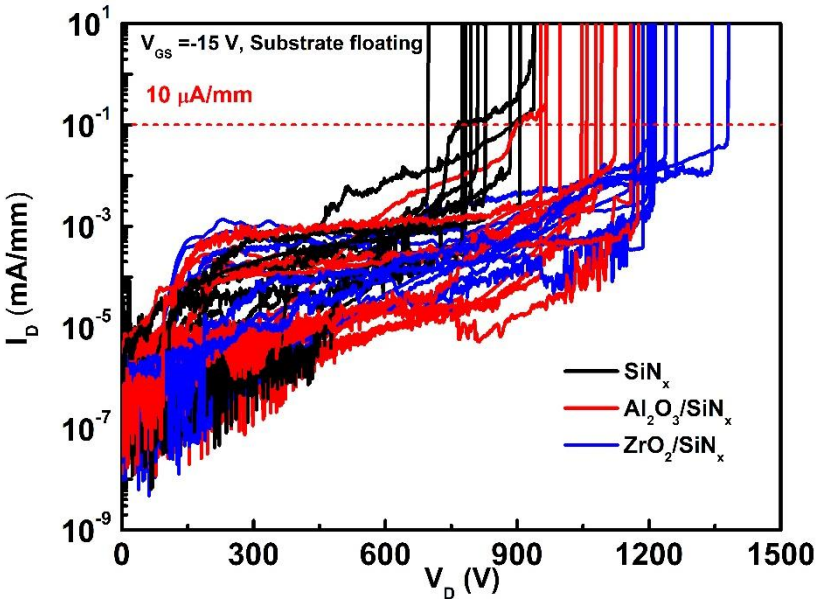

Fig. 4.20 Off-state breakdown characteristics of the fabricated samples with PECVD-SiN_x passivation (in 11 black lines), Al_2O_3/SiN_x passivation (in 11 red lines) or ZrO_2/SiN_x passivation (in 11 blue lines).

The off-state I_D-V_{DS} curves on 11 MIS-HEMTs have been randomly measured for each sample, the off-state breakdown characteristics curves of the 33 fabricated samples with different passivation layer are shown in Fig. 4.20. It can be observed that the drain leakage currents were equal to the gate leakage currents for all samples, this indicates the total leakage currents induced by the gate leakage currents. In addition, sample C with ZrO_2/SiN_x passivation exhibits a higher breakdown voltage which is the same as the result in the previous manuscript. The typical off-state breakdown voltage of three samples is extracted at V_{GS} = -15 V with the floating substrate. Sample A passivated by PECVD-SiN_x presents a breakdown voltage of 885 V, sample B with Al_2O_3/SiN_x passivation exhibits a breakdown voltage of 1092 V, which were extracted at drain leakage current criterion of 10 uA/mm. By contrast, for sample C with ZrO_2/SiN_x passivation, a higher hard breakdown voltage of 1207 V is observed, giving a power

figure of merit ($BV^2/R_{ON,sp}$) of 447 MW/cm^2. It is worth noting that the MIS-HEMTs with and without high-*k* dielectrics exhibited similar off-state drain and gate leakage performance, and the drain to gate leakage current dominated the off-state breakdown of devices.

A further 2-D electric field analysis was implemented by using Sentaurus TCAD simulation tools to explain why the actual devices with the high-*k* dielectrics passivation exhibit a higher breakdown voltage. The gate dielectric is a 20 nm Al_2O_3. The passivation layer is 100 nm thick and its relative permittivity (ε_r) is set as 4.2, 10, 20 and 30 in the simulation evaluation. The donor concentration in the AlGaN barrier and GaN channel layer is set at a low value of 1×10^{15} cm^{-3}. The devices are in an off-state, and their dimension is fixed as a 3 μm L_{SG}, a 3 μm L_G, and a 15 μm L_{GD}.

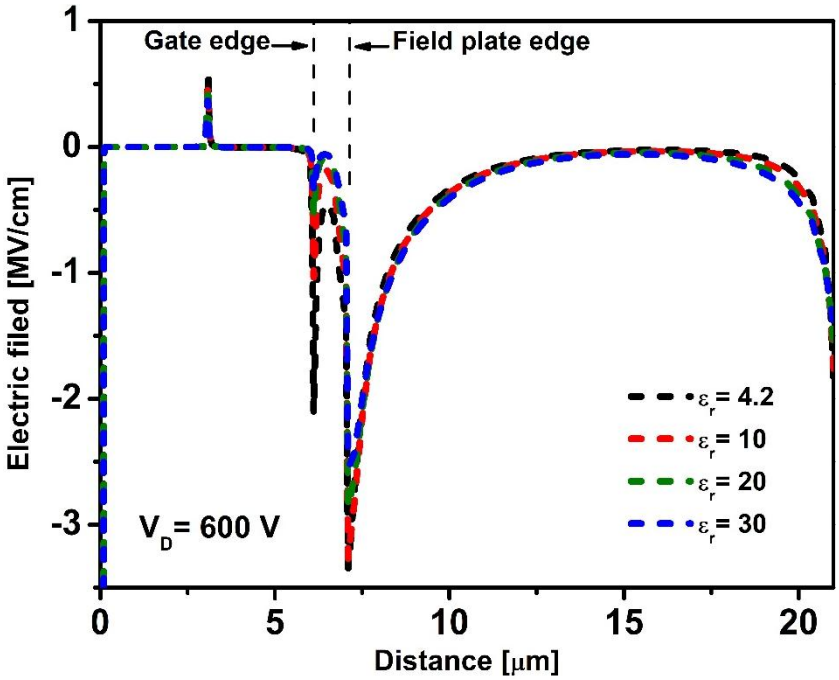

Fig. 4.21 Electric field profiles along AlGaN/GaN interface for a field plate length of 1 μm.

In the actual case, there was a 1 μm field plate-like hang at the drain side of the gate on the fabricated devices, which was used to avoid the alignment mistake during the photolithography process. Fig. 4.21 shows a comparison of electric field profiles at the AlGaN/GaN heterojunction interface for a 1 μm field plate at four cases with ε_r = 4.2, 10, 20 and 30. It can be observed that the field plate reduces the electric field peak at the drain edge of the gate significantly and causes a new electric field peak at the terminal of the field plate. In the case of ε_r = 4.2 (dashed line in black), the electric fields at the drain-electrode edge as well as at the field-plate edge become very high. By contrast, in the case of ε_r = 30 (dashed line in blue), the electric field profiles in these two regions are weaker. According to Gauss's law, the electric field across a dielectric is inversely proportional to its relative permittivity with a constant voltage applied on. For the devices when the high-*k* dielectrics passivated on the GaN, the electric field drop becomes weaker from the drain to the gate. It is explained that the devices with high-k passivation layers exhibited a higher breakdown voltage. The simulation results also indicated that the high-*k* passivation would not affect the field plates' function in modulating the electric field. In addition, a more uniform and weaker electric field distribution can be achieved from the drain to the gate for the case with the high-*k* passivation layer plus the field plate structure.

The experimental investigations on the high-*k* passivation have been started recently, but there have been few researches reported that how the high-*k* passivation layers affecting the high voltage properties of GaN-based MIS-HEMTs. Table 4.2 summaries the studies with high-*k* dielectrics passivated GaN-based MIS-HEMTs. It

seems that the breakdown voltage increased as ε_r increased, however, the effect of high-*k* dielectrics on suppressing current collapse is not clear. It is worth noting that the referenced studies are still mainly investigating those high-*k* dielectrics as the gate dielectrics on GaN-based MIS-HEMTs.

Table 4.2 A summary of experimental studies using high-*k* passivation layers on GaN-based MIS-HEMTs.

Reference	[25]	[28]	[7]	[23]	This work	This work
Year	2014	2019	2018	2019		
Dielectric	Al_2O_3/AlN	HfO_2	ZrO_x	$HfSiO_x$	Al_2O_3	ZrO_x
Permittivity ε_r	~9	~20	~28	~20	~7.5	~20
Breakdown voltage (V) L_{GD}= ~15 um	600	580	1084	~1100	939	1170
R_{ON} degradation ratio (@ 150 V Drain bias)	1.1	N.A	~1.1	1.3	1.14	1.25

In Fig. 4.22, a benchmark of the breakdown voltage versus the specific on-resistance of the three samples were presented and compared with other reported gate recess free GaN-based MIS-HEMTs [2-4, 22, 24, 29-32]. Samples A, B and C exhibited a specific on-resistance ($R_{ON,SP}$) of 3.31 mΩ•cm^2, 3 mΩ•cm^2 and 3.26 mΩ•cm^2, respectively, taking a 3 μm transfer length for source and drain ohmic contacts into account [33]. The $R_{ON,SP}$ is calculated by using the following equations,

$$R_{ON,SP} = R_{ON} \times W_G \times (L_{DS} + 3\ \mu m) \quad (4.1)$$

where R_{ON} is extracted from the DC I_D-V_{DS} output curves, W_G is the gate width and L_{DS} is the drain to source spacing. The fabricated AlGaN/GaN MIS-HEMTs with the ZrO_2/SiN_x passivation in this Chapter exhibited a satisfactory breakdown characteristic compared with other mainstream reports of the GaN-based MIS-HEMTs. Note that, although insertion of the high-*k* interlayers is capable of improving the high power performances of GaN-based devices, the additional step of ALD is required to be added into the fabrication process, which would increase the costs of devices fabrication. Further work will be focused on growing the high quality high-*k* dielectrics with a large thickness by using rapid deposition techniques.

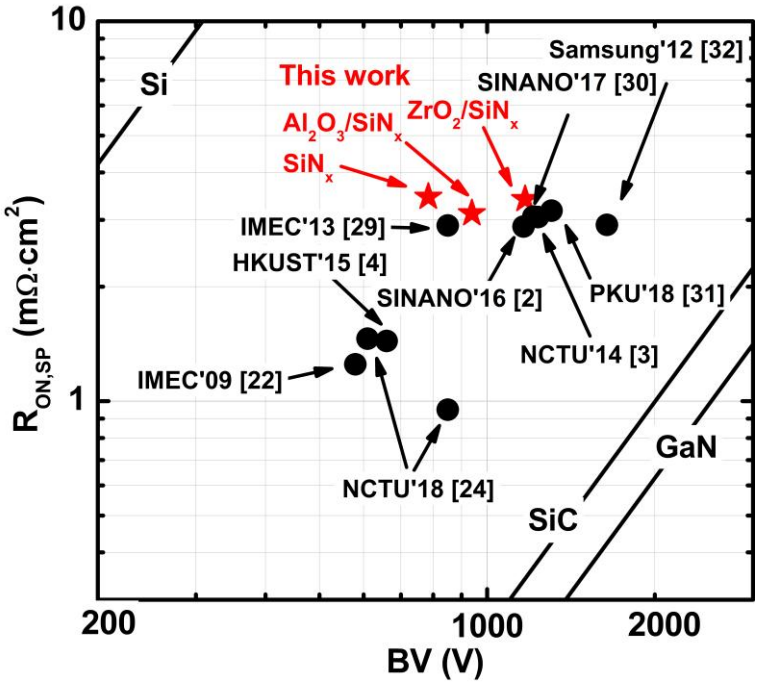

Fig. 4.22 Benchmark of breakdown voltage (BV) versus specific on-resistance ($R_{ON,SP}$) for devices in this work and state-of-the-art gate recess free GaN-based MIS-HEMTs.

4.5 Summary

In this Chapter, the AlGaN/GaN MIS-HEMTs with SiN_x single-layer passivation or with high-*k* dielectrics/SiN_x bilayer passivation are demonstrated and compared. The Al_2O_3/SiN_x passivated MIS-HEMTs present a breakdown voltage of 939 V, and the ZrO_2/SiN_x passivated MIS-HEMTs present a further high breakdown voltage of 1170 V. Moreover, switching after an off-state $V_{DS,Q}$ stress of 150 V, the current collapse effect of the high-*k* dielectrics/SiN_x passivated devices are significantly suppressed. This points out that the surface state on GaN can be passivated by the robust ALD dielectrics effectively. The results show a remarkable improvement in the breakdown and dynamic characteristics compared with the PECVD-SiN_x passivated MIS-HEMTs. In addition, a 2-D TCAD simulation of electric field profiles in the off-state MIS-HEMTs has been made, where the devices with various relative permittivity of the passivation layer are analyzed. The simulation analysis points out that the high-*k* passivation is capable of reducing the electric field intensity at the drain edge of the gate in MIS-HEMTs, thus improve the breakdown characteristic. The measured breakdown performance is in accordance with the simulated result, indicating that the breakdown characteristics of MIS-HEMTs can be improved by increasing the relative permittivity of the passivation layer. This shows a significant potential of employing ALD high-*k* dielectrics as the passivation layer on the GaN-based devices for high voltage switch applications.

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CHAPTER 5 A novel method for high voltage normally-off GaN MIS-HEMTs with low resistance

5.1 Introduction

In Chapter 4, the GaN-based MIS-HEMTs have been demonstrated as promising devices for the high voltage switching applications, owing to superior advantages of high breakdown electrical field, high current density, and fast switching speed. In power circuit applications, normally-off GaN-based HEMTs are preferred for safety consideration. Several approaches have been explored for realizing the normally-off operation of devices, such as fully recessed gate [1], thin AlGaN barrier [2], p-type GaN [3], fluorinated-gate [4], and oxide charge engineering [5]. The devices combing fully recessed gate with high-quality gate dielectric techniques [6] demonstrate the normally-off operation and good V_{th} stability, but the current density is low owing to the damaged 2DEG channel. Even though the p-type GaN normally-off devices [7] exhibit low on-state resistance, the low V_{th} and the low gate breakdown voltage are two significant imperfections. The E-mode devices with fluorinated-gate [8] demonstrate very high V_{th}, however, the device lack enough stability evidence. Thus, a novel technology is still expected for the commercialization of GaN normally-off power devices.

The GaN-based MIS-HEMTs using charge storage gate structure have been proposed to forward shift the V_{th} to achieve normally-off operation without large current degradation. A simulation analysis [9] indicated that the negative charges in a

floating gate or an oxide layer are capable of depleting the 2DEG beneath the gate region, resulting in a normally-off operation. In addition, some experimental studies reported that the normally-off MIS-HEMTs could be realized by using charge storage structure, such as the TaN floating gate [10], the HfO_2 charge storage layer [11], and the Al_2O_3 charge storage layer [12]. Furthermore, a high V_{th} normally-off MIS-HEMT with high drain current density by the combination of ferroelectric and charge storage layers have been demonstrated [13]. Even though the reported MIS-HEMTs with charge trapping structure achieved outstanding normally-off device properties, the complex gate structures, and the limited charge storage capacity are still important issues for the high voltage devices fabrication and applications.

In the first part of this Chapter, the realization of normally-off AlGaN/GaN MIS-HEMTs is demonstrated by using the fully recessed gate structure. The fully-recessed MIS-HEMTs exhibit an E-mode operation with satisfied sub-threshold characteristics. However, the low current density and large on-states resistance are two significant limitations for high power applications. Afterward, the deposition of the ZrO_x charge trapping layer on the partially recessed AlGaN in conjunction with the Al_2O_3 gate dielectric was developed. The deployment of the ZrO_x layer is capable of trapping abundant electrons after a positive gate bias initialization, which depletes the 2DEG beneath to realize the devices with E-mode operation. The electrical properties of normally-off AlGaN/GaN MIS-HEMTs with the ZrO_x charge trapping layer is demonstrated, which exhibit highly desired performance including positive V_{th}, high current density, high I_{ON}/I_{OFF} current ratio, high off-state breakdown voltage, and small

current collapse effect.

5.2 The detailed fabrication process of the normally-off GaN MIS-HEMTs

The investigated GaN HEMT structure consists of a 2 nm undoped GaN cap layer, a 22 nm thick $Al_{0.25}Ga_{0.75}N$ barrier layer, a 330 nm GaN channel layer, and a 5.1 μm GaN buffer layer on the silicon substrate. The fabrication processes of the MIS-FETs with fully recessed gate structure were started from the mesa isolation by using BCl_3/Cl_2 gas reactive ion etching. Then, the Au-free source and drain were formed by e-beam evaporation of Ti/Al/Ti/TiN (22.5/90/50/70 nm), and annealed at 870 ℃ in N_2 ambient for 40 s by rapid thermal annealing. The AlGaN barrier layer beneath the gate area was partially removed by 65 cycles of low power O_2 plasma oxidation and HCl-based oxide removal. The low damage digital etching with an etching rate of 0.4 nm/cycle is beneficial to control the etching depth precisely. The gate recess depth was ~26 nm according to the AFM measurement result. The SiN_x passivation layer was deposited by PECVD at 350 ℃ with an NH_3 flow of 10 sccm, a SiH_4 flow of 13.5 sccm and an N_2 flow of 1000 sccm. After the Si_3N_4 layer in gate regions was etched away by reactive ion etching, a 16 nm Al_2O_3 was then grown by ALD as the gate dielectric. The Al_2O_3 layer was deposited at 230 ℃ by using Trimethylaluminum (TMA) and H_2O as precursors of Al and oxygen, respectively, with an Al_2O_3 growth rate of ~0.11 nm/cycle. The thickness of dielectric films was evaluated from the best fit from spectroscopic ellipsometry

measurements. Finally, the devices were finished with Ni/TiN (50/100 nm) gate metal formation. A schematic cross-sectional view of the fabricated MIS-FETs fully-recessed gate structure is plotted in Fig. 5.1.

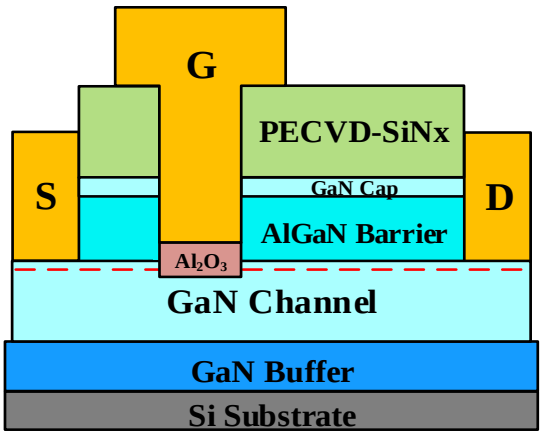

Fig. 5.1 Cross-sectional schematic of the fabricated MIS-FETs with a fully-recessed gate structure.

Similar to the MIS-FETs with a fully-recessed gate structure, the fabrication processes of the MIS-HEMTs with a ZrO_x charge trapping layer were started from the mesa isolation, and ohmic contact formation. The AlGaN barrier layer beneath the gate area was partially removed by 40 cycles of digital etching. The gate recessed depth was ~16 nm according to the AFM measurement result. After the surface clean processes on the wafer, a 4 nm Al_2O_3 tunneling layer was deposited on the wafer. Then, a 16 nm of ZrO_x charge trapping layer was deposited on the Al_2O_3 thin film. The ZrO_x layer was grown by ALD at 300 ℃. Tetrakis (ethylmethylamino) zirconium and H_2O were used as precursors of Zr and oxygen, respectively, with a ZrO_x growth rate of ~0.1 nm/cycle. Specifically, the pulse time of Tetrakis (ethylmethylamino) zirconium is 130 ms, the pulse time of H_2O is 50 ms, and the purge time is 30 s for these two precursors. The SiN_x passivation layer was deposited by PECVD at 350 ℃ with an NH_3 flow of 10 sccm, a

SiH_4 flow of 13.5 sccm and an N_2 flow of 1000 sccm. After the Si_3N_4 layer in gate regions was etched away by reactive ion etching, a 12 nm Al_2O_3 was then grown by ALD as a barrier layer to suppress the gate leakage current. The Al_2O_3 layer was deposited at 230 ℃ by using Trimethylaluminum (TMA) and H_2O as precursors of Al and oxygen, respectively, with an Al_2O_3 growth rate of ~0.11 nm/cycle. The thickness of dielectric films was evaluated from the best fit from spectroscopic ellipsometry measurements. Finally, the devices were finished with Ni/TiN (50/100 nm) gate metal formation. Fig. 5.2 shows a schematic cross-sectional view of the fabricated MIS-HEMTs with a ZrO_x charge trapping layer.

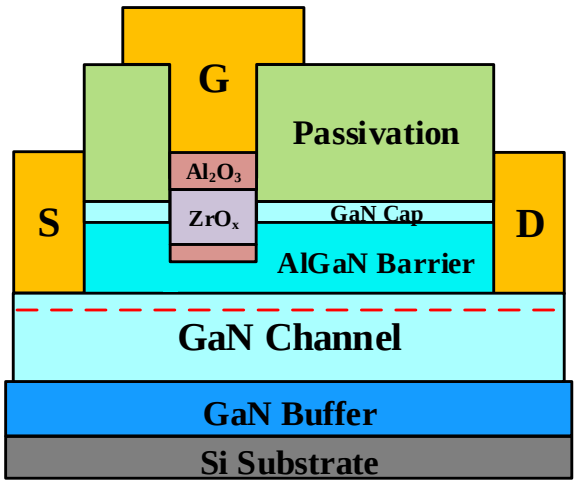

Fig. 5.2 Cross-sectional schematic of the fabricated MIS-HEMTs with a 16 nm ZrOx charge trapping layer and a 16 nm Al_2O_3 barrier gate stack.

5.3 DC I-V characterization on the gate fully-recess MIS-FETs and the MIS-HEMTs with ZrO_x charge trapping layer

The DC I-V characterization on the devices consists of the output & transfer characterizations, time-dependent dielectric breakdown (TDDB) characterization, fast switching on-state resistance characterization, and off-state breakdown voltage characterization. The output & transfer characterizations were firstly carried out on the gate fully-recess MIS-FETs. Fig. 5.3 shows I_D-V_{GS} characteristics of the AlGaN/GaN MIS-FETs with a source-gate distance L_{SG} of 5 μm, a gate length L_G of 3 μm, and a gate-drain distance L_{GD} of 5 μm. The devices exhibit a V_{th} of 2.27 V at drain the current criterion of 1 μA/mm and a well pinched-off at the off-state, indicating an actual E-mode operation. Moreover, a high I_{ON}/I_{OFF} current ratio (10^9), a suppressed gate leakage, a satisfied subthreshold slope S.S (~115 mV/dec), and a low V_{th} hysteresis (40 mV) are all achieved. This is because a high quality of Al_2O_3/GaN interface is formed by using the digital etching and ALD techniques.

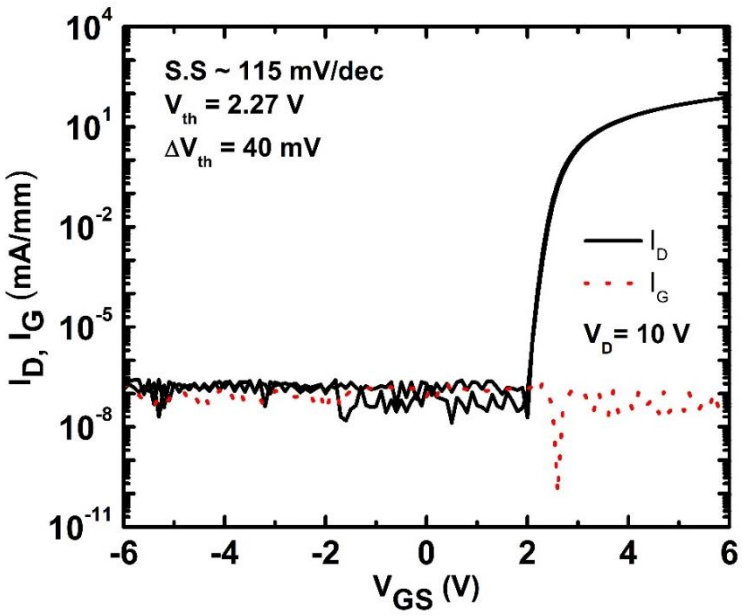

Fig. 5.3 Transfer and gate leakage characteristics of the gate fully recessed MIS-FETs at V_{DS} of 10 V in the semilog scale.

Fig. 5.4 shows I_D-V_{DS} & I_G-V_{DS} characteristics of the AlGaN/GaN MIS-FETs, where V_{GS} was swept from -6 to 6 V with a step of 3 V and V_{DS} was swept from 0 to 10 V. The maximum saturation drain current (I_{DS-max}) is extracted 64 mA/mm at V_{GS} = 6 V. The ON-resistance (R_{ON}) is 42.2 Ω·mm under V_{GS} = 6 V and V_{DS} = 0.25 V. Note that, the Ohmic contact is extracted to be 2 Ω·mm, indicating a very large resistance (38.2 Ω·mm) exhibited on the 13 μm conduction channel. The large R_{ON} on the conduction channel is possible due to the over-etching of the AlGaN barrier, and a part of the GaN channel layer has been etched. The electron conduction channel is located at the Al_2O_3/GaN interface in this case. Note that, the electron mobility at the Al_2O_3/GaN interface is much lower than that at the AlGaN/GaN 2DEG channel. Though a high quality of Al_2O_3/GaN interface can be achieved by using the digital etching techniques, the limited electron mobility at the Al_2O_3/GaN interface still results

in a significant degradation on the on-state resistance [14]. This motivates me to fabricate an E-mode GaN MIS-HEMTs but keeping the low-resistance AlGaN/GaN 2DEG conduction channel.

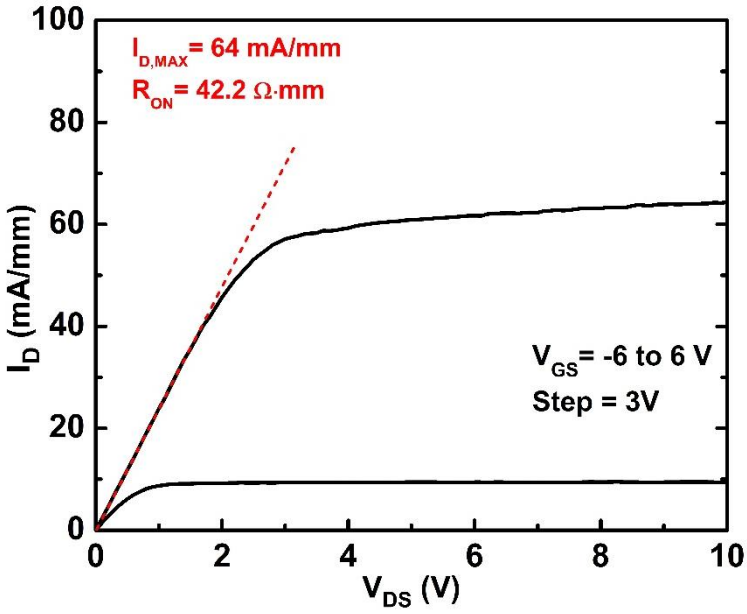

Fig. 5.4 Output characteristics of the gate fully recessed MIS-FETs

The relationship between the AlGaN barrier recess depth and the transfer characteristics was investigated on the fabricated Al_2O_3/AlGaN/GaN MIS-HEMTs with different recess depths. The AlGaN barrier recess depth beneath the gate region was measured as 0, 5 nm, 10 nm and 15 nm by using AFM. The transfer characteristics of the MIS-HEMTs with different recess depths at V_{DS} = 1 V are plotted in Fig. 5.5. It can be observed that the V_{th} of the devices forward shifts as the recess depth increases, and the maximum drain current at a constant gate bias decreases as the recess depth increases. Moreover, the slope of the I_D-V_{GS} slightly decreases as the recess depth increases, indicating the degradation of transconductance.

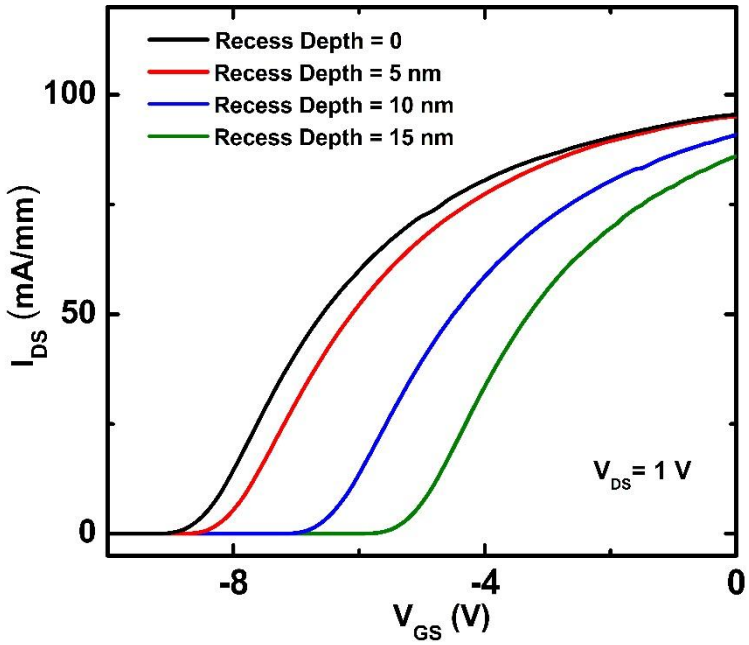

Fig. 5.5 The transfer characteristics of the MIS-HEMTs with different recess depths

For the fabricated MIS-HEMTs with a charge trapping layer, the gate recess depth was selected as ~16 nm for assisting a forward shift on V_{th} and for avoiding the degradation on output current at the same time. The I_D-V_{GS} characterizations were then carried out on the partial gate recessed the MIS-HEMTs with a 4 nm Al_2O_3 charge tunneling layer, a 16 nm ZrO_x charge trapping layer and a 12 nm Al_2O_3 barrier gate stack. The transfer characteristics of the fresh MIS-HEMTs (line in black) and the initialized MIS-HEMTs (lines in red and blue) with V_{DS} = 1 V are plotted in Fig. 5.6. The fresh devices exhibited D-mode operation with a V_{th} of −8.25 V. The initialization process was carried out by applying a high voltage of 12 V on the gate for 1 min. The initialized transfer curves were measured by the gate voltage double-direction sweeping between 0 V and 9 V with a step of 100 mV. The V_{th} was shifted to 1.51 V after the initialization process, at a drain current criterion of 1 μA/mm, which validates the

presence of negative charges in the gate stack layer. A V_{th} difference of nearly 9.76 V between the E-mode and D-mode operation implies an enormous potential of charge storage capacity. The devices exhibited a transconductance of 30 mS/mm, a threshold hysteresis -32 mV, a subthreshold slope (S.S) of 90 mV/dec and an I_{ON}/I_{OFF} ratio of ~10^8. The devices were well pinched off at V_{GS} = 0 V, indicating a normally-off operation. Moreover, the gate leakage was lower than 27 nA/mm at a high V_{GS} of 12V, implying the robust Al_2O_3 barrier is capable of suppressing the electron tunneling from the ZrO_x charge trapping layer to the gate electrode.

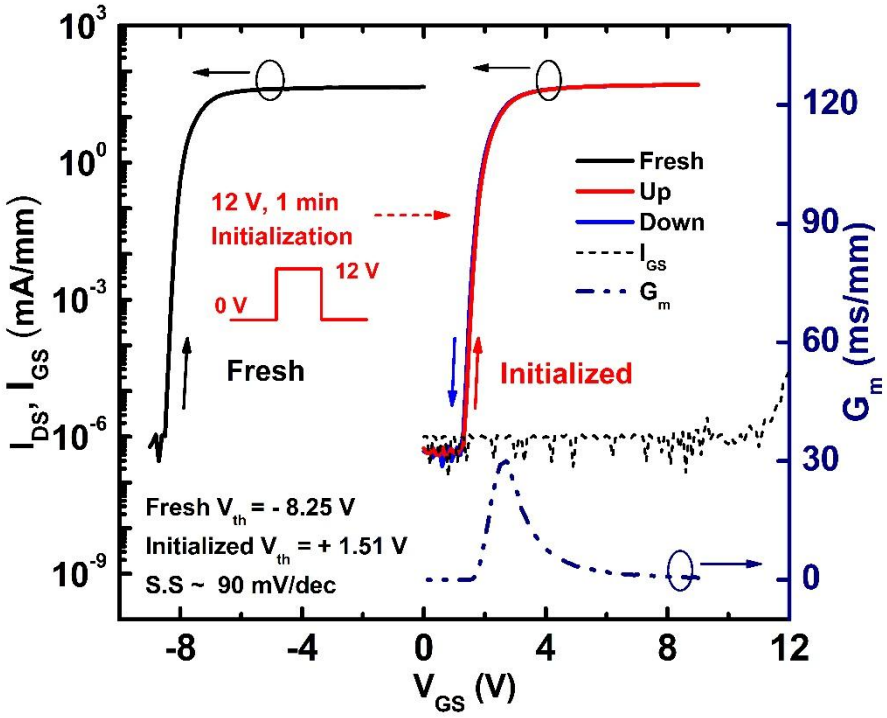

Fig. 5.6 Transfer characteristics of the devices with a 4 nm Al_2O_3/16 nm ZrO_x/12 nm Al_2O3 gate stack.

gate stack.

The TCAD simulation was carried out to understand the charge trapping behaviors and the effect of trapped charges in the MIS-HEMTs. Fig. 5.7 illustrates the

simulated schematic band diagrams of the metal/Al_2O_3/ZrO_x/Al_2O_3/AlGaN/GaN gate stack before, during, and after the 12 V initialization process. As shown in Fig. 5.7(a), in the fresh devices, the shallow bulk traps in the ZrO_x layer are empty due to the deep Fermi level. Here, the potential well (2DEG channel) is existed at the AlGaN/GaN interface due to the polarization effect. The conduction bands of the gate dielectric stacks keep moving toward the Fermi level with V_G increases. As shown in Fig. 5.7(b), during the 12 V initialization process, the nearly-flat potential of the AlGaN layer leads to the electron spilling-over from the 2DEG channel, and the electron would tunnel through the 4 nm thin Al_2O_3 layer due to a high electric field. After the electron comes into the ZrO_x charge trapping layer, the electron would be trapped in the high density bulk traps in the ZrO_x. At the same time, the 12 nm Al_2O_3 barrier layer would stop the electron tunneling to the gate and suppress the gate leakage current. After removal of the gate bias, the initialization has finished. Here, the bulk traps in the ZrO_x layer are still filled due to a relatively high conduction band offset (~ 1.15 eV) between Al_2O_3 and ZrO_x thin films, and the 4 nm Al_2O_3 layer works as a barrier layer to stop the electron de-trapping from the shallow bulk traps. It is worth noting that the filled bulk traps in the ZrO_x layer act as negative fixed charges. As shown in Fig. 5.7(c), these high density negative charges are capable of bending the conduction bands to a higher potential, and then deplete the 2DEG at AlGaN/GaN interface at a gate bias of 0 V.

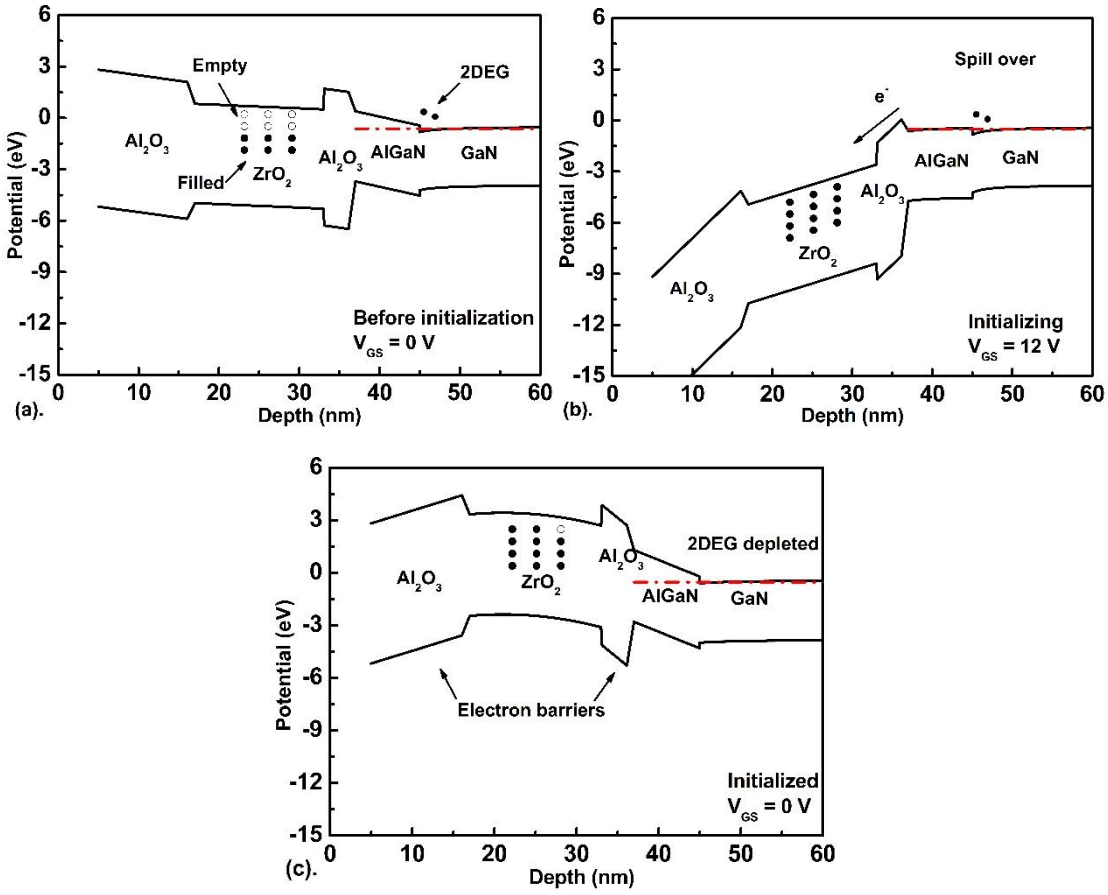

Fig. 5.7 The simulated schematic band diagrams of the metal/Al_2O_3/ ZrO_x/Al_2O_3/AlGaN/GaN gate stacks (a) before, (b) during, and (c) after the 12 V initialization process.

Fig. 5.8(a) and (b) illustrate the simulated diagrams of the electron density in the MIS-HEMT structure before and after the 12 V initialization process. It can be observed that the 2DEG channel beneath the gate region has been depleted in the initialized device (shown in Fig. 5.8(b)). Fig. 5.8(c) extracted the electron density at the gate cross profile of MIS-HEMTs before (line in black) and after the initialization process (line in red). Here, a high density (over 4e13 cm^{-2}) of electron is observed at the AlGaN/GaN interface for the fresh device. By contrast, a much lower electron density (~5e5 cm^{-2}) is extracted in the initialized device, which is not high enough to form a conduction

channel between drain and source electrodes. This indicates that the MIS-HEMT transfers from the normally-on operation to the normally-off operation after the 12 V initialization process.

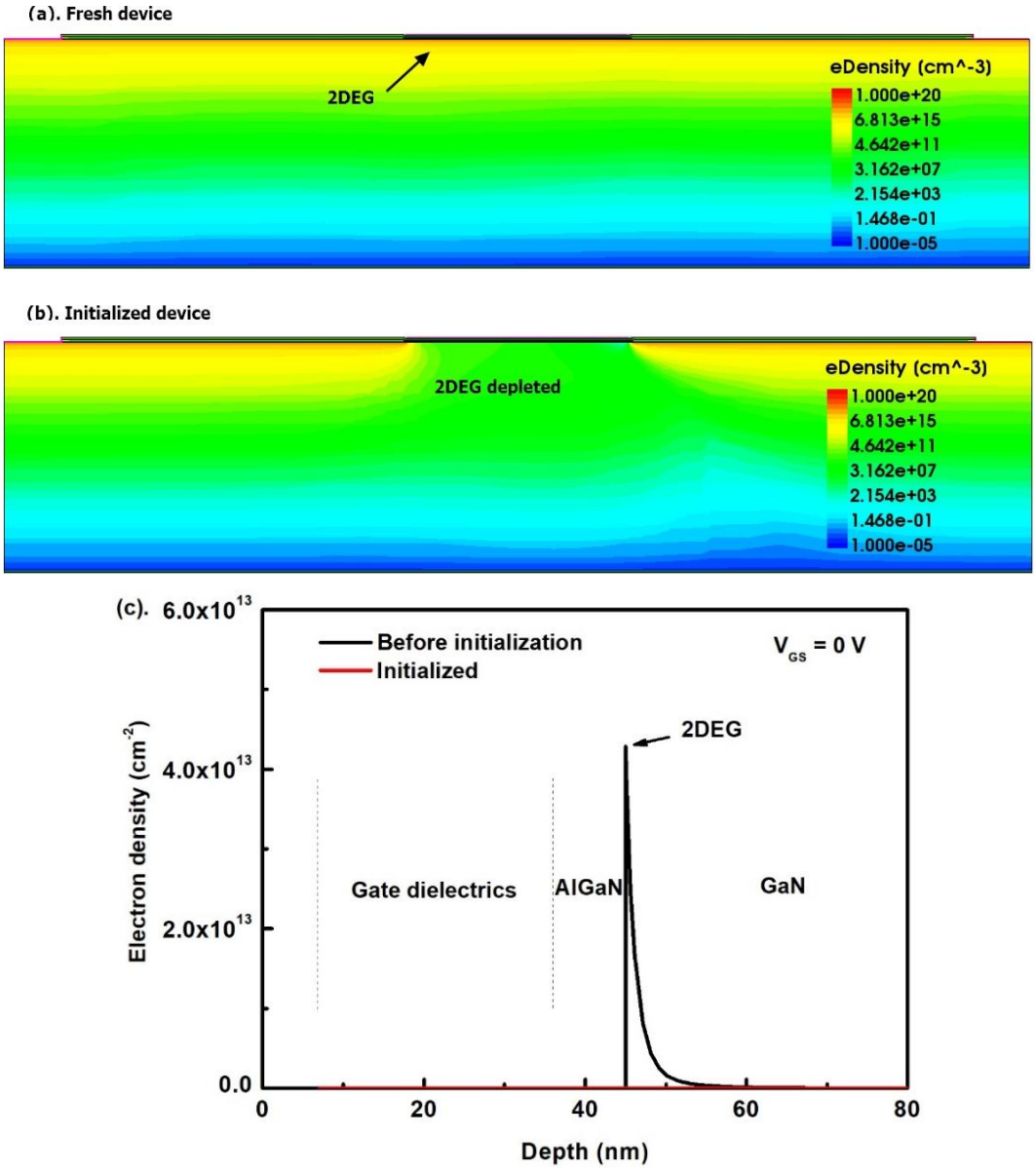

Fig. 5.8 The simulated diagram of the electron density in the MIS-HEMT structure at a gate bias of 0 V (a). before initialization process, (b). after initialization process, and (c). the extracted electron density at the gate cross profile of MIS-HEMTs before and after initialization process.

The V_{th} distribution histogram scatter diagram for 25 initialized MIS-HEMTs was plotted in Fig. 5.9. The V_{th} exhibited a narrow distribution with an average value of 1.51 V and a standard deviation of 0.21 V, which indicates an excellent uniformity of the charge storage structure.

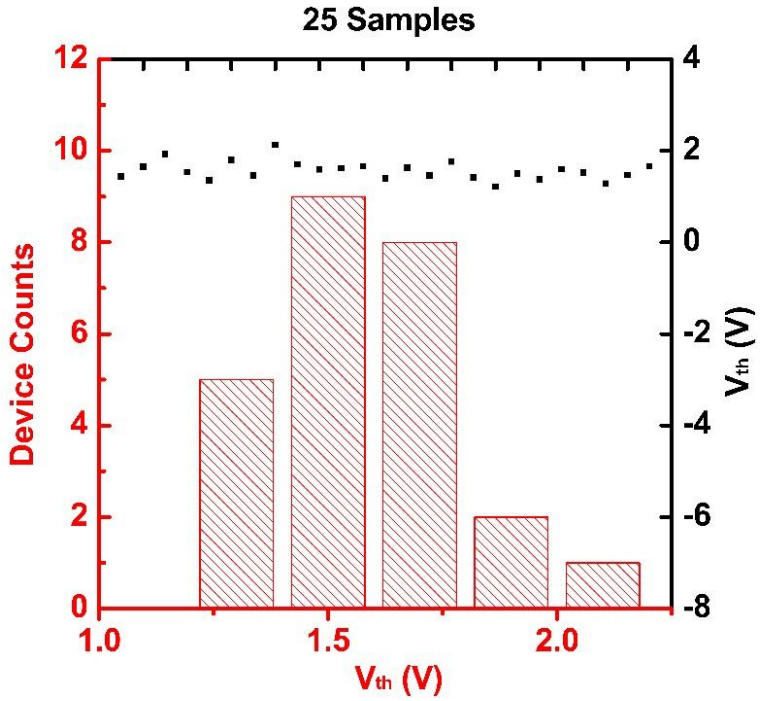

Fig. 5.9 Threshold voltage uniformity of 25 initialized E-mode MIS-HEMTs

The voltage drops on the gate structure during the 12 V gate bias initialization process was estimated for investigating the electron trapping location in the Al_2O_3/ZrO_x gate stack. When a 12 V bias is applied on the gate, the conduction band of AlGaN is pulled down below the Fermi level at the ZrO_x/AlGaN interface, resulting in the spillover of the electrons from 2DEG to the ZrO_x/AlGaN interface. This indicates that the voltage drop in the AlGaN layer was negligible. The voltage drops on the gate oxide stack (V_{ox}) can be calculated as,

$$qV_G = qV_{ox} + \Delta E_{C(Ni/Al2O3)} - \Delta E_{c(ZrO2/AlGaN)} \quad (5.1)$$

$$\Delta E_{C(Ni/Al2O3)} = \Phi_{Ni} - \chi_{ox} \quad (5.2)$$

$$qV_{ox} = qV_{Al2O3} + qV_{ZrOx} + \Delta E_{c(Al2O3/ZrOx)} \quad (5.3)$$

where $\Delta E_{C(Ni/Al2O3)}$ is the Schottky barrier between gate metal Ni and Al_2O_3, Φ_{Ni} = 5.1 eV is the work function of Ni and χ_{ox} = 1 eV is the electron affinity of Al_2O_3 [15], hence $\Delta E_{C(Ni/Al2O3)}$ is calculated to be 4.1 eV. $\Delta E_{C(ZrOx/AlGaN)}$ = 1.1 eV is the conduction band offset between ZrO_x and AlGaN. Base on the formulator in Eq. (5.1), the V_{ox} is calculated to be 13 V. According to Gauss's law, the voltage drops on the Al_2O_3 and ZrO_x were inversely proportional to their relative permittivity (ε_r). The ε_r of Al_2O_3 and ZrO_x in this work were measured as ~8 and ~18, respectively. ΔE_{C2} = 1.15 eV is the conduction band offset between Al_2O_3 and ZrO_x. The voltage drop on the Al_2O_3 is calculated to be ~6.75 V and the voltage drop on the ZrO_x is calculated to be 3.7 V. Therefore, during the 12 V gate bias initialization process, the sum of voltage drops on the Al_2O_3 and bandgap offsets is calculated to be ~9 V.

Another D-mode MIS-HEMTs with a 16 nm Al_2O_3 gate dielectric had been fabricated for investigating the electron trapping behavior in the Al_2O_3 barrier layer. Fig. 5.10 shows the transfer characteristics of the D-mode MIS-HEMTs before and after a 9 V gate bias. A forward V_{th} shift of 2.3 V was observed, indicating only a small density of electron concentration was trapped in the Al_2O_3 barrier layer or the interface between Al_2O_3 and GaN. It also suggests that the ~9.76 forward V_{th} shift observed on the MIS-HEMTs with a floating gate structure was mainly attributed to a high density of electrons trapped in the ZrO_x charge trapping layer.

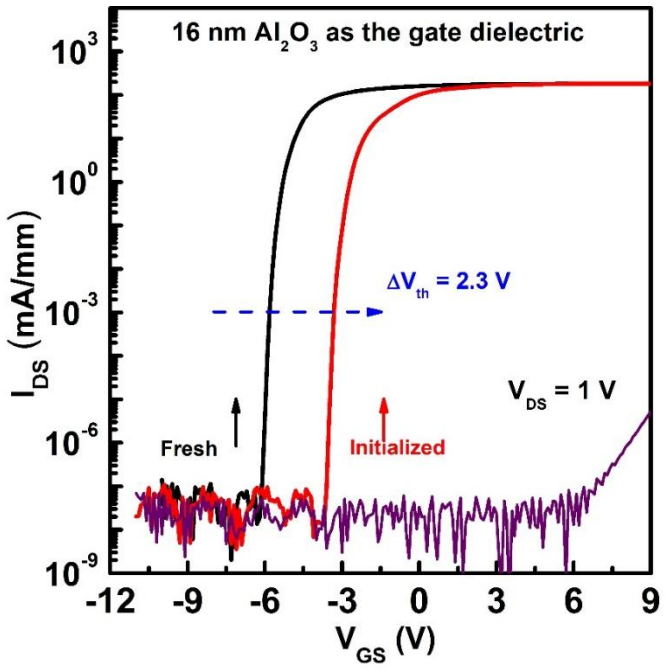

Fig. 5.10 Transfer characteristics of the D-mode devices with a 16nm Al_2O_3 gate dielectric before and after a 9 V gate bias initialization.

Here, it is important to point out the selection of ZrO_x as the charge trapping layer in this Chapter. The first important reason is the high charge storage capacity of the ZrO_x material. According to the calculation above, the ~9.75 forward V_{th} shift observed on the MIS-HEMTs with a floating gate structure was mainly attributed to a high density of electrons trapped in the ZrO_x charge trapping layer. Moreover, as illustrated in Fig. 5.7, the large conduction band offset between ZrO_x and Al_2O_3 (~ 1.15 eV) is another key reason. This high conduction band barrier is capable of suppressing the gate leakage current during the initialization process, and of avoiding the electron de-trapping from the shallow bulk traps.

The output characteristics of the initialized MIS-HEMTs are demonstrated in Fig. 5.11(a) where V_{GS} was swept from 0 V to 15 V with a step of 3 V and V_{DS} was swept from 0 V to 15 V. Here, the devices feature a L_{SG} of 3 μm, a L_G of 2 μm and a L_{GD} of 3

μm. The maximum drain current density was extracted to be 779 mA/mm at V_{GS} = 15 V. The on-resistance (R_{ON}) was 7 Ω·mm under V_{GS} = 15 V and V_{DS} = 0.25 V. Compared with the gate fully-recessed MIS-FETs with a large on-state of 42.2 Ω·mm (shown in Fig. 5.4), the partial gate recessed MIS-HEMTs with ZrO_x charge trapping layer exhibit a significant improvement on the output characteristics. The high output current density and low R_{ON} were well achieved owing to the damage-free of the AlGaN/GaN 2DEG channel. Note that, the Ohmic contact is extracted to be 1.7 Ω·mm, indicating a low resistance of 3.6 Ω·mm on the 2DEG conduction channel.

Fig. 5.12 benchmarks the $I_{DS, max}$ versus V_{th} of MIS-HEMT in this work with other state-of-the-art normally-off GaN-based devices. Our device exhibits a competitive positive V_{th} as well as a high density of $I_{DS, max}$. Not that, the R_{ON} of 7 Ω·mm in this work is a fairly small value compared with the normally-off devices in Fig. 5.12 with similar device dimensions. It clearly demonstrates the innovation to realize normally-off MIS-HEMTs by employing the ZrO_x charge trapping layer.

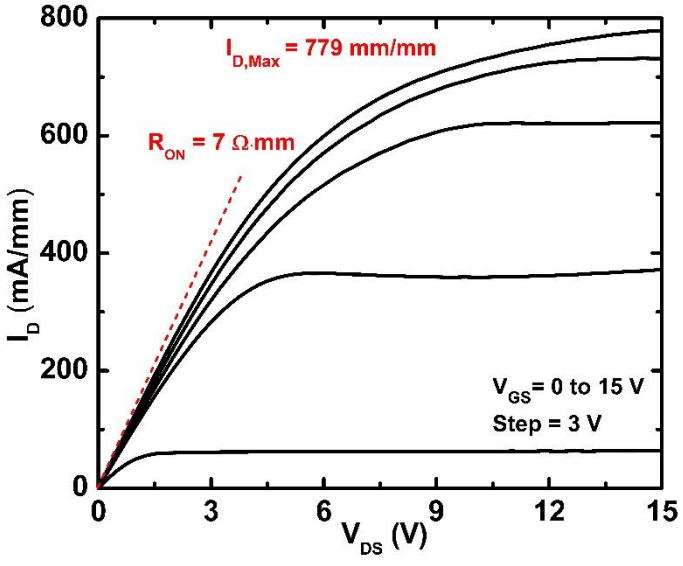

Fig. 5.11 I_D–V_{DS} characteristics of the MIS-HEMTs with L_{SG} = 3 μm, L_G = 2 μm, and L_{GD} = 3 μm.

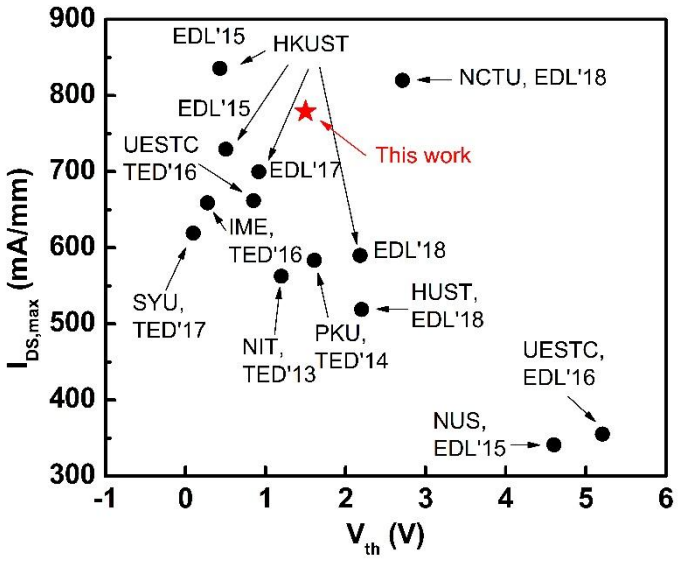

Fig. 5.12 Benchmarking of I_{DS}, max versus V_{th} for the state-of-the-art E-mode GaN transistors with an MIS gate structure. The V_{th} of the reference data was extracted from the transfer curve at I_D of 1 μA/mm.

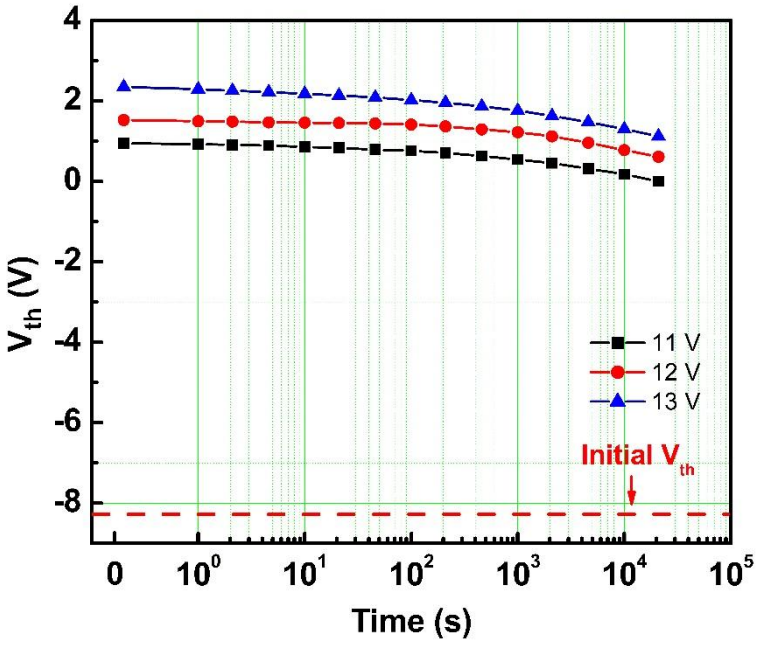

Fig. 5.13 Retention characteristics of the MIS-HEMTs after 11 V, 12 V and 13 V initialization processes.

The retention characteristics of the initialized MIS-HEMTs under static conditions at room temperature are shown in Fig. 5.13. All the electrodes were grounded between two V_{th} extractions. It can be observed that the V_{th} moves to a negative direction after

the initialization. In the case with a 12 V initialization (line in red), the total V_{th} shift presented a low value of -0.9 V. Here, the V_{th} was higher than 0 V for 21000 s indicating a weak charge de-trapping phenomenon, which due to a high conduction band off-set from the Al_2O_3 barrier to the ZrO_x. Note that, to ensure the safe normally-off operation of the devices, the initialization voltage should not less than 12 V.

The time dependent dielectric breakdown (TDDB) lifetime prediction is one of the most important indicators to evaluate the gate structure reliability of the MIS-HEMTs. The TDDB tests were performed at constant high forward V_{GS} bias of 14, 15, 16, and 17 V at room temperature (gate hard breakdown voltage was ~19 V) with source and drain grounded, respectively. The gate leakage current was recorded with time was shown in Fig. 5.14.

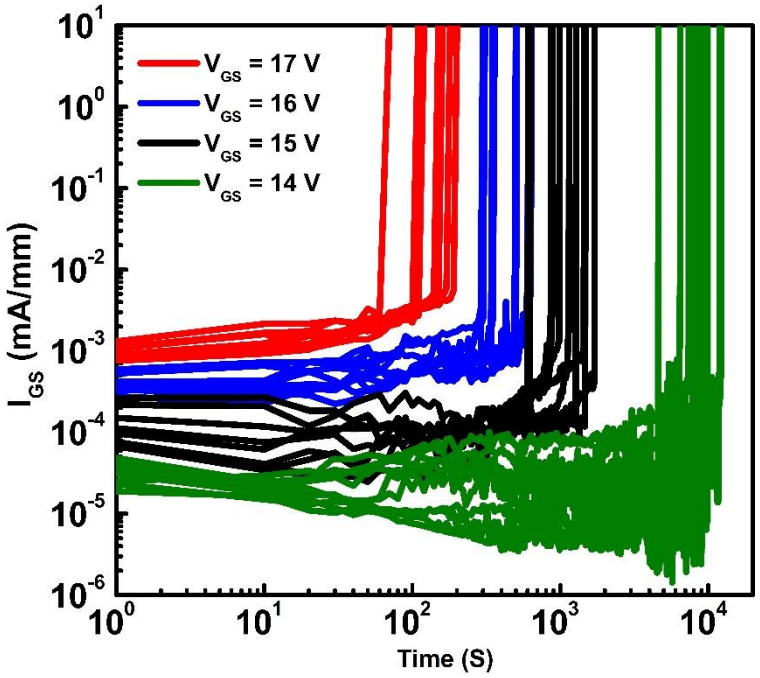

Fig. 5.14 t_{BD} of the MIS-HEMTs at gate stress of 14, 15, 16, and 17 V.

The breakdown time (t_{BD}) was defined when the suddenly increase in gate leakage.

The t_{BD} for gate dielectric degradation is commonly considered as following the Weibull distribution, which can be expressed as,

$$\mathrm{F(t)} = 1 - \exp\left[-\left(\frac{t-\gamma}{\eta}\right)^{\beta}\right] \quad (5.4)$$

where *t* is the lifetime, β is the destruction parameter, η is the scale factor, and γ is the time delay. Assumed γ equals to 0, the Weibull distribution function was expressed as:

$$\ln[-\ln(1-F(t))] = \beta\ln(t) - \beta\ln(\eta) \quad (5.5)$$

where a plot of the $\ln[-\ln(1-F(t))]$ versus $\ln(t)$ yields a straight line with a Weibull slope of β. This is capable of representing the statistic distribution and variability, a higher value of β indicates a more uniform statistic distribution of t_{BD}. For the devices with Al_2O_3/ZrO_x stack gate structure, t_{BD} of a constant stress voltage shows a Weibull distribution with β = 3.6, as shown in Fig. 5.15, indicating a small variability in breakdown time distribution [16]. In Fig. 5.16, the maximum V_{GS} is predicted to be 7.5 V for a 10-year lifetime of gate oxides stake at a failure level of 63% by using a combined TDDB model [17]. The combined TDDB model consists of the gate leakage current dominated by the PF emission at low electric fields and the gate leakage current dominated by the FN tunneling at high electric fields. In other words, the PF model was employed at low V_{GS} and the FN model was employed at high V_{GS}. For the PF model, the breakdown time is described in the $\sqrt{E}$ model [18], (as shown in Eq. 5.6) For the FN model, the breakdown time is described in the 1/E model [19], (as shown in Eq. 5.7)

$$t_{BD} = Exp\left(-\alpha\sqrt{E_{ox}}\right) \quad (5.6)$$

$$t_{BD} = Exp\left(\frac{\beta}{E_{ox}}\right) \quad (5.7)$$

where α and β are parameters.

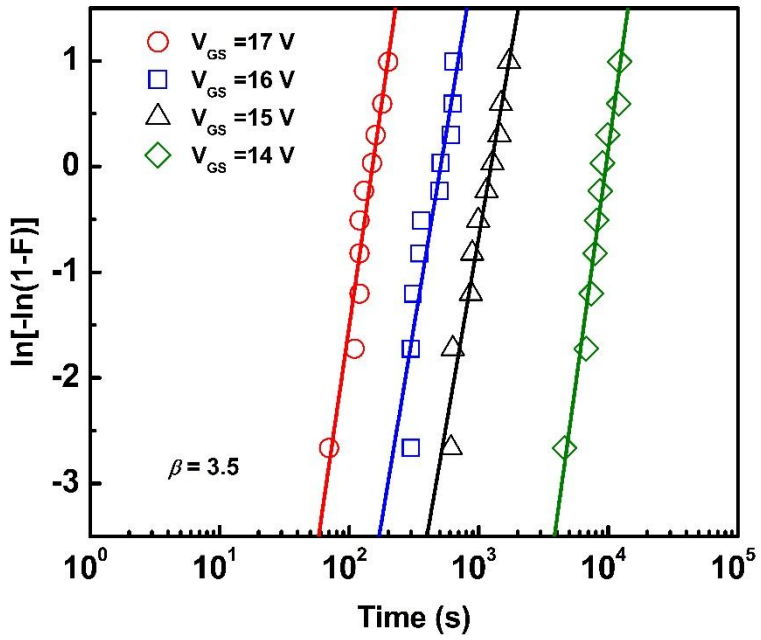

Fig. 5.15 Weibull plot of the electric field-dependent t_{BD} distribution.

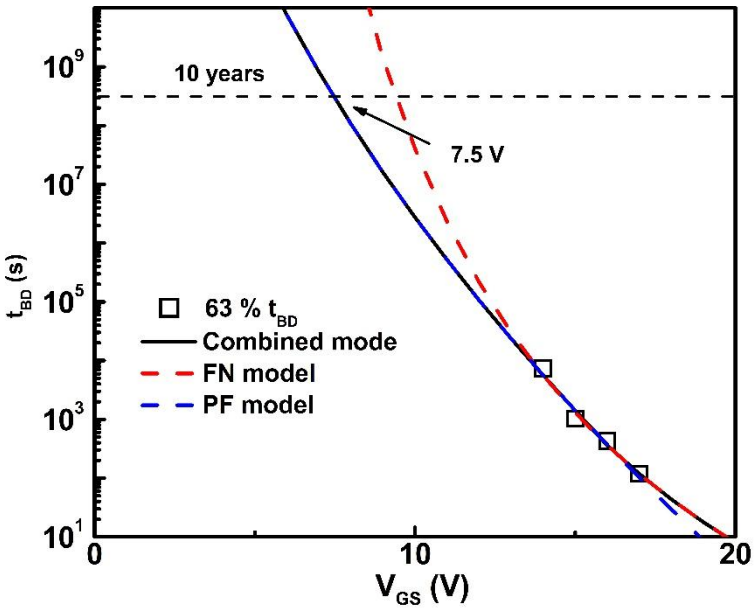

Fig. 5.16 Lifetime prediction of the 63% failure level using combined TDDB models over a wide range of field.

The dynamic on-state performance of the devices was evaluated by using a pulsed I_D-V_{DS} measurement under fast switching with different quiescent bias points. Here, the devices feature an L_{GD} of 15 μm. The quiescent gate bias ($V_{GS, Q}$) was fixed at -9 V, the

off-state stress time was 2 s, and the off-state to on-state switching time was 500 μs. The DC and pulsed I_D-V_{DS} curves were shown in Fig. 5.17 (a) that were measured at V_{GS} = 15 V. The ratio of dynamic R_{ON} ($R_{ON,D}$/ $R_{ON,S}$) was plotted in Fig. 5.17 (b), and the R_{ON} here were extracted at V_{DS} = 0.25 V. The devices exhibit a negligible degradation of $R_{ON,D}$ for quiescent drain bias lower than 75 V, and the $R_{ON,D}$/ $R_{ON,S}$ is 1.5 when the off-state stress $V_{DS,Q}$ is 200 V. The results demonstrate a suppressed current collapse compared with the devices in Chapter 4 with PECVD-SiN_x passivation, suggesting the ALD-ZrO_x passivation layer could suppress shallow interface traps or protect the GaN surface from the plasma damage.

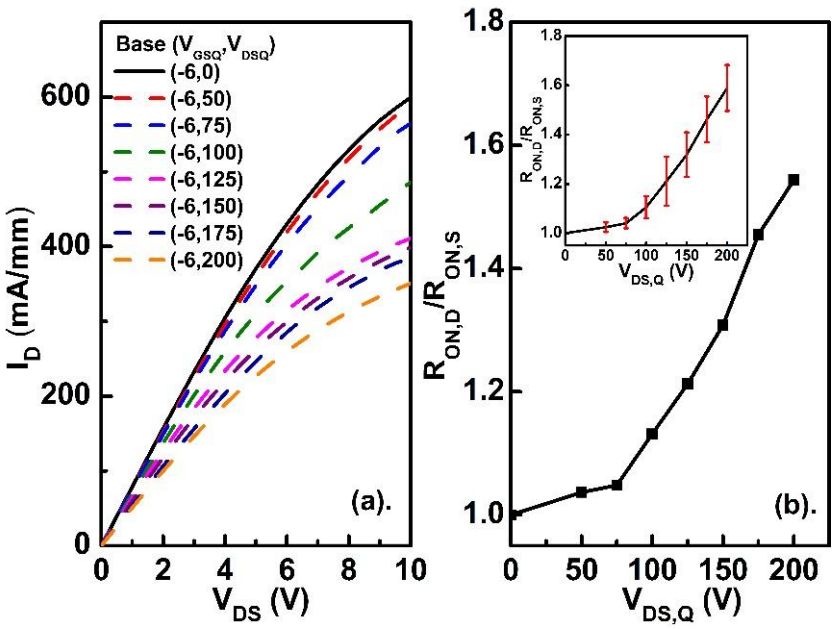

Fig. 5.17 (a) Behavior of current collapse of the MIS-HEMTs measured at different quiescent bias points. (b) Ratio of the dynamic on-resistance over the static one ($R_{ON,\ D}/R_{ON,\ S}$) of the MIS-HEMTs at different quiescent drain bias points. (Inset figure: The means value and the standard deviation of $R_{ON,\ D}/R_{ON,S}$ at different quiescent drain bias points)

Fig. 5.18 (a) plots the off-state breakdown characteristics of MIS-HEMTs at a V_{GS} of -9 V with the floating substrate. Fig. 5.18 (b) plots the L_{GD}-dependent breakdown voltage (BV) and specific on-resistance ($R_{ON,SP}$). The breakdown voltage increases with L_{GD} spacing is observed. This is because as drain voltage increases to the breakdown voltage, the electric field at the drain side increases. It is important to point out that electrons and holes are generated by impact ionization due to a high electric field, particularly at the drain edge of the gate. The generated electrons flowing to the drain and gate electrodes would cause a sudden increase in the drain and gate leakage currents and leading to the direct device breakdown. The increasing of L_{GD} spacing is capable to reduce the electric field intensity between the drain and the gate, hence the breakdown characteristics improved. However, the on-state resistance is increased at the same time as shown in Fig. 5.18 (b), it is important to notice that the trade-off between on-state resistance and breakdown voltage of the GaN-based MIS-HEMTs. The MIS-HEMTs with an L_{GD} of 20 μm exhibited a $R_{ON,SP}$ of 3.78 mΩ•cm^2. Moreover, a high breakdown voltage of 1447 V had been extracted at drain leakage current criterion of 10 uA/mm, indicating a power figure of merit ($BV^2/R_{ON,SP}$) of 554 MW/cm^2. As shown in Fig. 5.19, a benchmark of the breakdown voltage versus the $R_{ON,SP}$ of the devices was compared with other state-of-the-art E-mode GaN-based devices. The E-mode MIS-HEMTs with the ZrO_x charge trapping layer in this chapter exhibited an excellent breakdown and conduction characteristics compared with other mainstream reported GaN-based MIS-HEMTs.

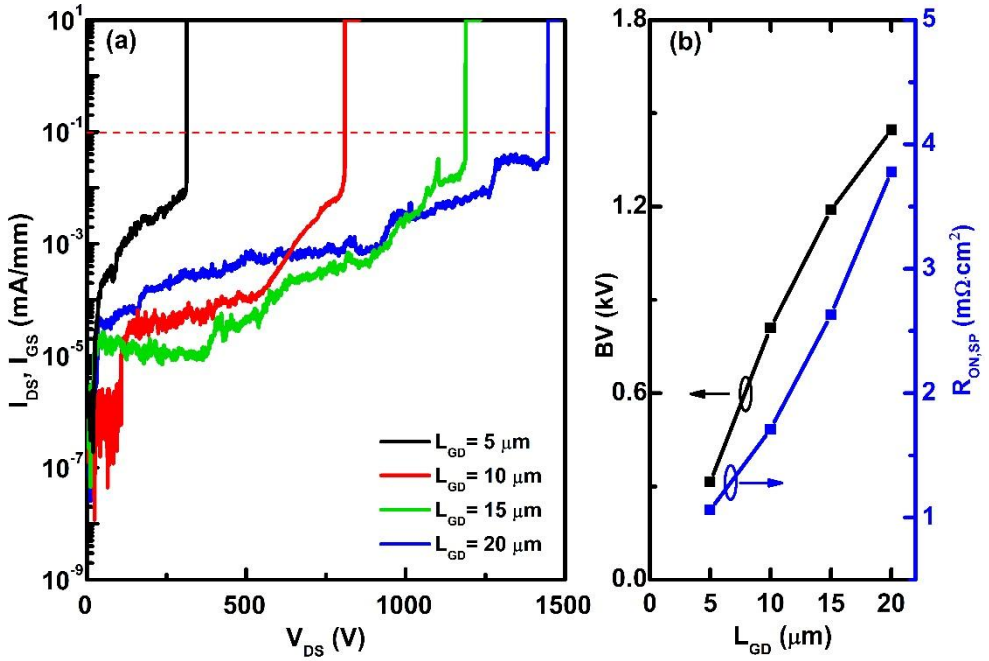

Fig. 5.18 (a) Breakdown characteristics of the fabricated AlGaN/GaN MIS-HEMTs with different L_{GD} values. (b) L_{GD}-dependent breakdown voltage and on-resistance of the MIS-HEMTs.

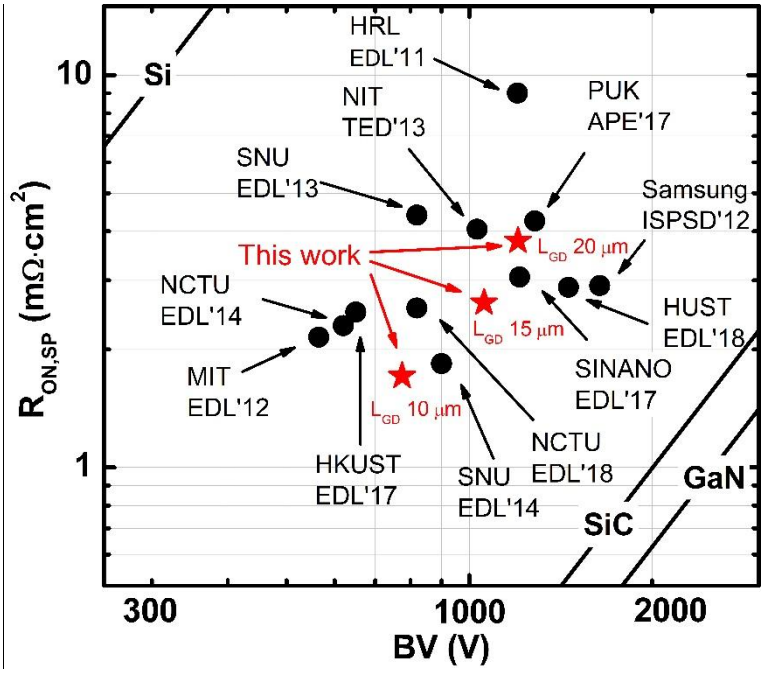

Fig. 5.19 Benchmarking of BV versus $R_{ON,SP}$ for devices in this work and state-of-the-art normally-off GaN-based MIS-HEMTs.

5.4 Summary

In this chapter, the normally-off gate fully-recess MIS-FETs and the normally-off AlGaN/GaN MIS-HEMTs with ZrO_x charge trapping layer beneath gate are demonstrated. The normally-off gate fully-recess MIS-FETs exhibit a positive V_{th} of 2.27 V and satisfied subthreshold characteristics. However, a maximum drain current density of 64 mA/mm, which accompanied a large on-resistance of 44.2 Ω·mm. The significant degradation of the on-state resistance is caused by the over-etching of the 2DEG channel. For the normally-off AlGaN/GaN MIS-HEMTs with the ZrO_x charge trapping layer, the ALD-ZrO_x layer enables the E-mode operation owing to the storage of negative charges. The fabricated MIS-HEMTs presented a threshold voltage of 1.51 V and a maximum drain current density of 779 mA/mm, which accompanied a low on-resistance of 7 Ω·mm. In the V_{th} retention test, the V_{th} was all higher than 0 V for 21000 s indicating a weak charge de-trapping phenomenon. In addition, a tight gate dielectric breakdown time distribution and small variability in breakdown behavior are achieved. The maximum V_{GS} bias is predicted to be 7.5 V for a 10-year lifetime at a failure level of 63%. Moreover, switching after an off-state $V_{DS,Q}$ stress of 200 V, the degradation of dynamic on-resistance was a low value of 1.5, indicating a satisfactory interface between oxide passivation and GaN. Furthermore, the devices exhibit a high breakdown voltage of 1447 V. Though further improvement is needed on the charges storage stability, the results indicate a significant potential of employing the ALD-ZrO_x charge trapping layer to realize normally-off the GaN-based devices for high power switching applications.

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Chapter 6 Conclusions and Future Work

6.1 Conclusions

In this study, the simulation, fabrication and characterization of AlGaN/GaN MIS-HEMTs were focused on realizing normally-off devices with high breakdown voltage and low on-state resistance. The achieving of the target devices was accomplished in the sequence of reducing the gate dielectric/GaN interface states density, improving the off-state breakdown voltage, and realizing the normally-off operation. The fabricated devices exhibited a positive V_{th} of +1.51 V, a high breakdown voltage of 1447 V, and a high output current density of 779 mA/mm, which offered a possible solution for the high-power applications.

In Chapter 3, studies on achieving reliable AlGaN/GaN MIS-HEMTs and reducing the gate dielectric/GaN interface states were carried out. The TCAD simulation was first implemented to understand the effect of gate dielectric parameter and Al_2O_3/GaN interface states on the C–V behavior of AlGaN/GaN MIS-capacitors. It was found that a higher Al_2O_3/GaN interface state density would cause a more forward shift on the V_{th} and a more stretch out on the C–V curves. After that, the MIS-devices without treatment or with HCl, O_2 plasma, and ODT surface treatments were demonstrated and compared. According to the XPS analysis, the re-oxidation on the GaN surface is difficult to avoid by using the acid-based surface treatments. In addition, the O_2 plasma and ODT treatment are capable of passivating the GaN surface by oxygen atoms and sulphur atoms, respectively, which may fill the N vacancies and defects. The electrical

characteristics pointed out that the O_2 plasma treatment reduced the positive charges on the GaN surface and suppressed the positive bias-induced V_{th} instability considerably. In contrast, The MIS-HEMTs with the ODT surface treatment exhibited a more suppressed Al_2O_3/GaN interface state density and satisfied sub-threshold characteristics. The studies in this chapter provided a reliable MIS gate structure scheme for achieving GaN-based devices with low drain/gate leakage currents and stable DC I-V characteristics.

In Chapter 4, the simulation of off-state electric field profiles in the MIS-HEMTs as functions of the structure of devices was carried out. One important simulated result pointed out that using high-*k* passivation is capable of reducing the electric field intensity at the drain edge of the gate in MIS-HEMTs, hence improve the breakdown voltage. Based on the simulation analysis, the AlGaN/GaN MIS-HEMTs with PECVD-SiN_x single-layer passivation or with high-*k* dielectrics/SiN_x bilayer passivation were demonstrated and compared. Compared with the SiN_x passivated devices, the devices with high-*k* passivation exhibited a suppressed off-state leakage current. Moreover, the current collapse effect of the high-*k* dielectrics passivated devices was significantly suppressed, owing to the effective passivation of the shallow traps on the GaN surface. In addition, the Al_2O_3/SiN_x passivated MIS-HEMTs presented a breakdown voltage of 1092 V, and the ZrO_2/SiN_x passivated MIS-HEMTs presented a further high breakdown voltage of 1207 V. The measured breakdown performance was in accordance with the simulated results, indicating that the breakdown characteristics of MIS-HEMTs can be improved by increasing the relative permittivity of the passivation layer. This indicated

a remarkable improvement of the breakdown and dynamic characteristics compared with the PECVD-SiN_x passivated MIS-HEMTs. The high-*k* dielectrics passivated devices with high breakdown voltages and suppressed dynamic degradations offer a possible option for high voltage switch applications.

In Chapter 5, firstly, the normally-off AlGaN/GaN MIS-FETs with a fully-recessed gate structure was demonstrated. The gate fully-recessed MIS-FETs exhibited a truly normally-off operation (V_{th} = 2.27 V) and satisfied subthreshold characteristics. However, the maximum drain current density was only 64 mA/mm, which accompanied a large on-state resistance of 44.2 Ω·mm. The significant degradation of the output performance is caused by the over-etching of the 2DEG channel. In order to improve the on-state conductivity, a novel normally-off AlGaN/GaN MIS-HEMTs with combining the partial gate recess structure and the ZrO_x charge trapping layers in conjunction with Al_2O_3 layers were proposed. The fabricated AlGaN/GaN MIS-HEMTs presented a stable threshold voltage of +1.51 V and a maximum drain current density of 779 mA/mm. The accompanied on-resistance of 7 Ω·mm is a relatively low value compared with the up-to-date mainstream studies. In the V_{th} retention test, the V_{th} was all higher than 0 V for 21000 s indicating a weak charge de-trapping phenomenon. In addition, a tight gate dielectric breakdown time distribution and small variability in breakdown behavior were achieved. The maximum V_{GS} bias was predicted to be 7.5 V for a 10-year lifetime of gate oxides stack at a failure level of 63%. Moreover, the degradation of dynamic on-resistance was a low value of 1.5 at a $V_{DS,Q}$ of 200 V, indicating a satisfactory interface between ALD-Al_2O_3 and GaN. Furthermore, the

devices exhibited a high breakdown voltage of 1447 V indicating a significant potential of employing the ALD-ZrO_x charge trapping layer to realize normally-off the GaN-based devices with high breakdown voltage and low on-state resistance. The studies in this chapter provided a novel device structure scheme for high power applications.

6.2 Future Works

In conclusion, this thesis provided a possible option for the future application of GaN-based devices in power electronics. The normally-off AlGaN/GaN MIS-HEMTs with high breakdown voltage and low on-state resistance have been fabricated successfully; however, further works are still needed to be carried out.

Firstly, the ODT surface treatment techniques can be further improved by optimizing the concentration of the ODT solution, the treatment temperature, and the alkane chain removal methods. The carbon contamination caused by the ODT surface treatment is an important imperfection of this technique.

It is also suggested to carry out a more accurate extraction on the onset voltage during the dielectric/GaN interface state calculation by using a multi-frequency C-V method. The onset voltage needs to be evaluated at a specific capacitance where the traps at the interface that are modulating; however, this specific capacitance is extracted by a low-error estimation at present.

Moreover, it is also possible to find other substance dielectrics as the passivation of GaN-based MIS-HEMTs. According to the measured results in Chapter 4, though a

relatively low state density of ~10^{12} $cm^{-2}eV^{-1}$ excites on the GaN surface by using Al_2O_3 passivation, the improvement of the breakdown voltage is not significant. In order to further improve the high voltage performance, it is possible to find another dielectric with a higher permittivity, and this dielectric is capable of passivating the GaN surface state more effectively at the same time.

Finally, in order to improve the V_{th} stability of the normally-off MIS-HEMTs with a charge trapping layer demonstrated in Chapter 5. The insertion of a tougher electron tunneling layer between the AlGaN barrier and the charge trapping layer can be researched in the future. The electron tunneling layer is able to let electrons tunneling through during the high gate bias initialization process and make electrons trapping more stable within the charge trapping layer after the gate bias is removed. This electron tunneling layer is suggested with a large conduction band offset to the charge trapping layer and a good interface quality toward the AlGaN barrier layer.